# KDF 8

# Programming Manual



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# I N D E X

# 1. GENERAL DESCRIPTION 1.

KDF 8 is a general-purpose Electronic Data Processing System specially designed for medium to large scale office data processing. Developed from the field-proven KDP 10 System which it replaces, KDF 8 provides a significant improvement in performance but retains the system and program compatibility features of its predecessor.

## 1.1 FEATURES OF THE SYSTEM

The following features of KDF 8 make it particularly suitable for commercial applications.

### 1.1.1 Completely Variable Data Organisation

The system is capable of accepting and processing alphanumeric data originating on punched paper tape, punched cards and magnetic tape. Information from each type of input medium is retained in the internal store in character form and every character is addressable. Special instructions in the order code permit the processing of variable length items and operands and it is not necessary to reserve space for maximum capacity items and messages. This ability to dispense with redundant padding characters, necessary in fixed word length machines, saves space on tape and in the high speed store and decreases processing time.

### 1.1.2 Addressable Registers

The registers used by the program control unit in the execution of orders are accessible to the programmer by the use of special instructions in the order code. The final contents of these registers helps the programmer to control variable length data operations.

### 1.1.3 Decimal Arithmetic

In addition to the normal binary arithmetic operations there are provided the four usual arithmetic operations which handle decimal information. Two variable length operands may be added, subtracted, multiplied or used in division operations.

### 1.1.4 Accuracy Checking

Built-in checking ensures the correct transfer of information between peripheral equipment and computer, and within the computer itself. Arithmetic operations are checked by repeat operations using the complements of the operands.

### 1.1.5 Simultaneous Operation

Time sharing of the control organisation by the input-output equipment and the processing circuits within the computer permit simultaneous operation of the following:-

a) Reading information from tape

b) Writing information on tape

c) Computing

1. General Description (Cont.) 1.

d) Operating High Speed Printer

1.1.6 Expansibility

The system is flexible and readily capable of expansion in terms of number of tape units, size of internal store and type of peripheral equipment.

1.2 CENTRAL PROCESSOR

The Computer is a digital machine in which information is stored in binary coded characters. Each character, whether on tape or within the computer, uses six information digits and a parity digit. Sequential control governs the order in which instructions are obeyed and normally one instruction must be complete before the next instruction starts. This, of course, does not apply to the simultaneous mode of operation where certain selected operations may proceed together. The use of a core store provides random access to internally stored information. A KDF 8 computer is made up from a selection of on-line units chosen from the following:-

a) High Speed Memory

b) Computer Program Control

c) Tape Selecting and Buffer Unit

d) Control Console

e) Monitor Printer

f) Paper Tape Reader

g) Line Printer (Model 1033 and 1040)

1.2.1

The HIGH SPEED MEMORY is a random access, magnetic core device which provides storage and work area for programs and data. The Memory is available in increments of 16,384 character locations and may be expanded to a maximum of 262,144 locations. Each location is individually addressable and can store any one of the sixty-four characters. These characters (KDF 8 Code) include all the letters of the alphabet, the ten decimal digits, control symbols and special marks. One character or four characters in parallel can be addressed, brought into the Memory Register and generated in their original locations in one 12.5 microsecond cycle.

1.2.2 The PROGRAM CONTROL is the arithmetic and logical control element of the Computer. It interprets and executes the instructions of the program stored in the High-Speed Memory and performs the automatic accuracy checks. The Computer and the on-line peripheral devices operate in accordance with a stored program of two-address instructions. The instructions that can be executed by the Program Control include all the categories necessary for processing of data: Input-Output, Data Handling, Arithmetic, and Decision and Control. Each instruction is made up of eight characters and consists of four parts: (1) an operation code (read, multiply, transfer, etc.)

(2) an A address (usually the High-Speed Memory address of an operand or the left boundary of an operand), (3) a B address (usually the High-Speed Memory address of an operand or right boundary), and an N code. The N code permits automatic modification of address A and/or B through the use of any of the seven (four static and three dynamic) Address Modifiers.

1.2.3 The TAPE UNITS and Model 1040 ON-LINE PRINTERS are connected to the Computer by Tape Selecting and Buffer Units-A, and are handled by the same instruction codes, thus permitting the Programmer complete flexibility in the handling of these devices, as well as permitting data to be transferred to the On-line Printer at rates comparable to Magnetic Tape speeds.

Writing from the Computer to Magnetic Tape Units and to Model 1040 Line Printers, and Reading to the Computer from Magnetic Tape Units, is at the rate of 40,000 characters per second.

The total of eight Tape Units and/or Model 1040 Printers directly controlled by the Computer may be increased to as many as sixty-two by connection of a TAPE SELECTING UNIT-B to each of the Unit-A trunk lines.

1.2.4 The CONSOLE provides for complete monitoring of operation of the Computer and the on-line devices with panel display and control of register and status level action. Automatic and manual operation, maintenance, program insertion and program testing can be accomplished from the Console.

Console facilities include:

1. Manual start and stop at a given instruction or at a given address.
2. Control and display of registers and counters.
3. Accuracy-checking indicators.
4. Indicators for currently-performed instruction.
5. Indicators for last or currently-selected Tape Unit.
6. Control and display of Character Recognition flip-flops.
7. Breakpoint switches.
8. Alarm indicators.

1.2.5 The MONITOR PRINTER is an on-line device, similar to an electric typewriter, that prints on paper stock from information received directly from the Computer's store. It operates at the rate of ten characters per second and is used primarily for program operational control, program testing, and exceptional types of output. The Paper Tape Punch associated with this device can produce seven-hole punched tape simultaneously with the Monitor Printer's output of hard copy.

### 1.2.6 Paper Tape Reading

The KDF 8 Paper Tape Reader accepts seven-hole punched paper tape and operates at the rate of 1,000 characters per second. It is used largely for initial program insertion, program testing, and insertion of periodically-changing constants, and also for the input of data.

### 1.2.7 High Speed Printing

High Speed Printing can be accomplished ON-LINE, or OFF-LINE, in the KDF 8 System.

The print-line capacity is 80, 120 or 160 characters and the print rate is up to 1,000 lines per minute.

The Model 1040 Printer operates in conjunction with a DATA EDITOR under the direction of a plugboard program and a paper tape loop, with information received either directly from the High Speed Memory, or via a magnetic tape mounted on its own, independent tape unit.

The Model 1033 Printer accepts data directly from the Computer Memory only, operating under the direction of the Stored program, and printing at 600 lines per minute.

## 1.3 ADDITIONAL EQUIPMENT

In addition to the equipment described above, the KDF 8 System includes a choice of peripheral off-line equipment comprising Card Transcriber, Tapewriter and Tapewriter Verifier. These are described in detail in the KDF 8 Functional Specifications and only brief descriptions are included here.

### 1.3.1 Card Transcriber

This comprises two units, a CARD READER and a CARD EDITOR. The Card Reader may be used without the Editor, in which case editing is reserved for the Computer. This device converts characters on eighty-column punched cards to coded characters on magnetic tape, at the rate of up to 425 cards per minute. The Card Reader includes a control panel, an automatic card-handling mechanism and two card-reading stations. Each card is read at both stations, and the readings are compared as an accuracy check. The Card Transcriber employs transistor circuitry, and accuracy control includes parity, comparison and multi-punch checks.

### 1.3.2 Tapewriter and Tapewriter-Verifier

These are used for original preparation and verification of coded, seven-hole punched paper tape for subsequent input to the Computer via the Paper Tape Reader. These devices are keyboard operated and simultaneously print on paper stock the same information that is being punched on tape. The Tapewriter-Verifier automatically checks the accuracy of its output by comparison with a previously prepared (Tapewriter) punched paper tape. Whenever a character being punched on the Tapewriter-Verifier is not in agreement with the related character on the original tape, both the keyboard and the punch lock. Both devices will function at typing speeds up to 10 characters per second, and both include parity checking.

## 1.4 SUMMARY OF EQUIPMENT PERFORMANCE

### ON-LINE EQUIPMENT

| | |
|---|---|
| Magnetic Tape | 40,000 characters per second Maximum. |
| Paper Tape | Input - 1,000 characters per second. |
| Monitor Printer | 10 characters per second with paper tape punched simultaneously. |
| High Speed Printer | 1,000 lines per minute. 80, 120, or 160 characters per line. |

### OFF-LINE EQUIPMENT

| | |
|---|---|
| Card Transcribed Card Reader | 425 cards per minute. |
| Tapewriter and Tapewriter Verifier | 10 characters per second. |
| High Speed Printer | 1,000 lines per minute. 80, 120, or 160 characters per line. |

## 1.5 ACCURACY CHECKING FEATURES

The KDF 8 design incorporates several accuracy checking features which aim to prevent incorrect information from entering or leaving the System. The provision of extra equipment for checking must be selective or there is a danger of overloading the System with so much extra equipment that further check circuits are required to check the original checking equipment. The following description indicates the techniques used and the area of application.

### 1.5.1 Parity Checking

Each character on magnetic tape and in the computer store carries an extra 'bit', or binary digit, to make the total number of '1' bits an odd number. On paper tape the number of '1' bits is an even number. Correct parity is ascertained on read-in, during computer operations and on write-out.

During read operations the characters are checked in the computer before they are stored in the HSM. On output operations the Tape Units are arranged to provide echo returns from the tape recording heads and so indicate whether a correct character has been written. Parity checking is equally important in the off-line equipment and is extensively used in card-to-tape and tape-to-card conversions and in the off-line printer.

### 1.5.2 Dual Recording on Magnetic Tape

The bits of each character together with a timing pulse are recorded in duplicate on sixteen channels across the width of the tape. All dually-recorded characters are read or written simultaneously and good characters from either track are accepted. By this means either one of the two recorded

spots for a single bit may be missing and the character still be read successfully. Failure to read a particular bit may occur through flaws in the tape or through deterioration of the tape after many passes through the tape unit. Dual recording, besides improving the accuracy of recording also lengthens tape life.

### 1.5.3 Repeated Operations

If a parity error occurs on tape during a read operation the tape is automatically returned to the beginning of the block or message and the read instruction repeated. If, on the second run, the same, or another parity error is detected the Computer stops and an alarm light indicates the reason for the stoppage. This feature is known as ROLL-BACK and further details are given later in this manual.

### 1.5.4 Arithmetic Checks

All additions and subtractions are checked by repeated operations using the complements of the operands, character by character. As decimal multiplication and division are performed by repeated additions and subtractions these operations also are checked. If agreement is not obtained the computer stops and indicates the cause of the stoppage. This checking does not increase the arithmetic operation times.

## 1.6 APPLICATION OF CHECKING TECHNIQUES

PROGRAM CONTROL The following conditions occurring within the Computer will cause the machine to stop:

Incorrect parity in Memory Address Register

Incorrect parity in Memory Register

Arithmetic Unit failure

Incorrect parity in Bus Adder

Invalid operand in a Decimal Operation

Incorrect parity in Normal Operation Register

Incorrect transfer of an operation from Normal to Simultaneous Mode

More than one Previous Result Indication

Failure of Time Pulses

INPUT OUTPUT EQUIPMENT The following input output conditions cause the Computer and input or output unit to stop:

Tape Unit detects signals in an Intermessage Gap or Interblock gap.

Missing Clock Pulse

Tape Unit control signals incorrectly obeyed.

Odd number of characters in a paper-tape block read.

Second parity error after Rollback.

Incorrect Tape Selection.

Incorrect data format, e.g. incorrect Start Message - End Message sequence.

Incorrect parity return from recording-head during a Tape Write operation.

Incorrect paper tape parity.

On-Line Printer not operable.

On-Line Printer paper supply low.

# 2. SUMMARY OF THE ENHANCED FEATURES OF KDF 8 2.

## COMPARED WITH KDP 10

### 2.1 CENTRAL PROCESSOR

The Central Processor of KDF 8 has a store cycle and status level time of 12.5μs, thus significantly decreasing the execution time of all instructions.

Moreover certain operations of a high frequency of occurrence have been accelerated even further:

#### 2.1.1 Instruction Modification.

This has been reduced to 25μs for each address modified.

#### 2.1.2 Three Character Add and Subtract Instructions.

These instructions, which in KDP 10 were primarily for address manipulation, are now performed in parallel, and are executed in 75μs including staticizing and STA time.

#### 2.1.3 Sector Compare Instruction Logic.

This logic has been enhanced to permit faster decisions to be made by commencing operations at the most significant end of operands, and terminating immediately inequality is discovered.

### 2.2 MAGNETIC TAPE UNITS

The MAGNETIC TAPE units of KDF 8, whilst retaining the same comprehensive features of KDP 10, now operate at 40,000 char./sec.

The 40,000 char./sec. units of KDF 8 are fully compatible with the 33,000 char./sec. units of KDP 10.

### 2.3 LINE PRINTER

A new LINE PRINTER, the MODEL 1040 replaces the 1035 (off line) printer. It may also be used in an on-line role as an alternative to the Model 1033 printer.

As well as having an increased print and paper skipping speeds in either role, (up to 1000 lines per minute on selected alphanumeric ranges), the on-line model has been enhanced also to be an asynchronous type to which data may be transferred at magnetic tape writing speeds, and which will print and advance paper in parallel with other operations.

Furthermore the device is handled by the same range of instructions as magnetic tape units, thus permitting full flexibility in the automatic (program) switching of devices.

The 1040 Line Printer is available with 80, 120, or 160 Print positions per line, and additional paper motion control facilities are provided. 54 different characters may be printed and 13 non printable characters provide control functions.

2. Summary of the Enhanced Features (Cont.) 2.

Due to the dual use of the symbol 0 as a numeral and alphabetic character, a total of 68 possibilities exists. The choosing of 64 of these is performed by the code select plug which is pre-wired for a particular use of the printer.

## 2.4 SIMULTANEOUS OPERATION

A Third Level of Simultaneity has been introduced to permit compute/read/write simultaneity. In conjunction with the introduction of the 1040 printer this means that compute/read/write/print simultaneity is also available.

### 2.4.1 Revised Instructions

The following Revised Instructions have been provided to operate in conjunction with the additional simultaneous mode:

62: Sense simultaneous mode

65: Sense simultaneous Gate 1

73: Store Register

75: Control simultaneous Gate 1

### 2.4.2 New Instructions

The following New Instructions have been provided to operate in conjunction with the additional simultaneous mode:

60: Sense simultaneous operations

64: Sense simultaneous Gate 2

74: Control simultaneous Gate 1 and 2

## 2.5 COMPATABILITY

Existing KDF 10 Programs can be run on KDF 8 with little, if any, modification.

# 3. KDF 8 SUPPLEMENT TO THE KDP 10 PROGRAMMING MANUAL 3.

This section should be read in conjunction with the KDP 10 Programming Manual, to which reference is made throughout.

## 3.1 TAPE UNITS AND LINE PRINTERS

The uprating of the transfer speeds of magnetic tape units does not involve any change in Instruction codes or characteristics.

However, the use of the model 1040 Printer in an on-line configuration calls for clarification.

Information to be printed is prepared and laid out as if it were being written to magnetic tape for use on an off-line Printer, and should be transferred to the device using tape writing instructions and the appropriate trunk number. Instructions so used will display the same Register and simultaneity characteristics.

Though certain functions will clearly be of no significance as far as the Printer is concerned (e.g., unwind/rewind n symbols), the Trunk Sense instruction has been revised to indicate the current state of the Printer when that device is designated.

## 3.2 SIMULTANEITY (TIME-SHARING OPERATIONS) ON KDF 8

In order to describe the Simultaneity features of KDF 8, it is necessary to understand the similar features of KDP 10.

These may be summarized thus:

Simultaneity in KDP 10 is defined as coincident execution of two instructions, both or one of which is an input-output instruction.

All instructions are staticized in the Normal Mode. Some instructions must be totally executed in the Normal Mode. All but three of the input-output instructions can be completed in either mode and are termed potentially simultaneous (PS) instructions.

A potentially simultaneous instruction automatically shifts (any time after it is staticized) into, and is then completed in, the Simultaneous Mode if that mode is unoccupied by a previous instruction and if the Simultaneous Gate is open. This permits initiation(in the freed Normal Mode) of the next instruction in sequence. The two instructions are then executed with total or partial coincidence in time (time-shared). The exceptions are that two 'read' instructions or two 'write' instructions cannot be executed simultaneously. If, for instance, a 'read' instruction is in process in the Simultaneous Mode and another 'read' instruction is staticized in the Normal Mode, the latter instruction is not executed until the instruction in the Simultaneous Mode has been completed.

Reading and writing may be accomplished simultaneously as long as the two instructions do not involve the same Tape Unit. If, for example, a 'read' from Tape Unit 20 is staticized while writing is in process at the Tape Unit, the 'read' will not be executed until writing has been completed.

Trunk $(77)_8$, however, can be time-shared by a paper tape 'read' and a 'write-out' to the Monitor Printer, but only if the 'write' to the monitor printer is staticised first.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

With the inclusion of an ADDITIONAL SIMULTANEOUS MODE on KDF 8, read/write/compute simultaneity may be achieved.

The Simultaneous mode of KDP 10 (now renamed SIMO 1, will allow the execution of READ instructions only, on KDF 8. The new simultaneous mode (SIMO 2) will permit only the execution of Linear Write* (To Line Printer or Tape Unit).

Existing Programs can operate without modification, but to make optimum use of this new facility some program revision may be desirable.

The degree of simultaneity (whether only one, or both, of the modes shall be active at any one time) is under Program control.

If Simultaneous Gate 1 is closed, all instructions will be performed serially in the Normal mode.

If Simultaneous Gate 1 is open and Simultaneous Gate 2 is closed, only two-way simultaneity will be possible as shown in the following chart:

| Normal Mode | Simo 1 | Simo 2 |
|---|---|---|
| COMPUTE | READ | |
| COMPUTE | | WRITE* |
| READ | | WRITE* |
| WRITE | READ | |

* Linear write (or Transcribing Card Punch Write).

It should be observed that Shutting Simultaneous Gate 2 does not inhibit Simo 2 completely, but only prevents its use simultaneously with Simo 1. The Programmer is thus provided with a means of controlling whether KDF 8 or KDP 10 simultaneity characteristics shall be in force at any time. This may also be controlled from the Console.

With both Simultaneous Gates open, three way simultaneity may be achieved. All computing operations may be performed in the normal mode, all read operations in Simo 1, and all Linear write instructions in Simo 2.

Provided the appropriate data transfer has been completed, the on-line Model 1040 Printer may, additionally, be printing or paper-advancing.

* NOTE: Transcribing Card Punch Write Instruction (now redundant) may also be executed in Simo 2 if used in error.

To achieve this enhanced simultaneity, certain Registers have revised characteristics, and some new Registers have been provided. Furthermore, certain instructions have been revised, and three new instructions are available.

Detailed descriptions are given in the Sections which follow.

## 3.3 KDF 8 REGISTERS

To exploit the increased simultaneous potential of KDF 8, additional Registers have been provided, and the function of some existing Register has been amended.

Those Registers of interest to the Programmer are shown below. New Registers, or Registers with amended functions are designated with an asterisk.

The MEMORY ADDRESSING REGISTER stores the HSM address of the tetrad to be processed. The capacity of this register is three characters (six octal digits).

The MEMORY REGISTER has a capacity of four characters. It receives the tetrad contents that emerge from or are to be placed in the High-Speed Memory. A series of MEMORY OUTPUT GATES permit or inhibit entrance into the Memory Register of any or all of the four characters that emerge from the HSM.

The P REGISTER holds the HSM address of the next instruction in sequence.

The A REGISTER has a capacity of three characters. It receives the A address of an instruction and, when necessary, holds the address of each character (or tetrad) being processed in the Normal Mode.

The B REGISTER has a capacity of three characters. It receives the B address of an instruction and, when necessary, holds the address of each character or tetrad being processed in the Normal Mode. When an instruction shifts from the Normal to the Simultaneous Mode, the B Register no longer holds the B address of the shifted instruction, but is utilized by the instruction which then occupies the Normal Mode.

The B address is not sent to the B Register in three of the forty-nine instructions: Transfer Control (71), Set Register (72) and Store Register (73).

* The S1 REGISTER is a three-character register used to hold the A address of a read instruction when the read is executed in the Simo 1 mode.

* The S2 REGISTER is a three-character register used to hold the A address of a write instruction when the write is executed in the Simo 2 mode.

* The SO REGISTER is a one-character register used to hold the operation code of the read instruction when the read is executed in the Simo 1 mode.

The T REGISTER has a capacity of three characters. It holds the third address when required by an instruction (e.g., HSM address for the quotient in a Decimal Divide Instruction). In some instructions it is used as an internal counter.

The NO (NORMAL OPERATION) REGISTER has a capacity of one character. It holds the Operation Code of the instruction currently being executed in the Normal Mode.

The N REGISTER has a capacity of one character. It holds the N character of the currently processed instruction.

The SR (SELECT READ) REGISTER has a capacity of one character. It holds the address of the input device used in a Read operation.

The SW (SELECT WRITE) REGISTER has a capacity of one character. It holds the address of the output device used in a Write operation. The SW Register is not used in the Print (On-Line Printer) instruction.

*The SC REGISTER is a one-character register used as temporary storage for Compute instruction (used in place of SR or SW Register). This register is also used for Break Point recognition on a transfer of control instruction and for decoding the Store Register and Set Register instructions.

ADDRESSABLE REGISTERS. A,B,P,S1,S2 and T are all addressable registers. Their contents may be conveniently set and/or stored for subsequent program reference.

## 3.4 LIST OF KDF 8 INSTRUCTIONS

Except as indicated below, instructions are exactly the same as the corresponding KDP 10 INSTRUCTIONS, and reference should be made to the KDP 10 Manual for details of unchanged instructions. In the description of new and revised functions given below, the asterisk references have the following meanings:-

* Indicates that the instruction has revised characteristics.

** Indicates that the instruction is an entirely new function. These instructions are fully described in Section 3.5 of this Publication.

*** Indicates that the instruction has revised potential simultaneity characteristics.

01: Program Error Stop (PES)

This instruction inhibits the staticising of any further instructions, halting the Computer after completion of any instruction in the Simultaneous Modes and illuminating an alarm light on the Computer Console.

02: * Print (PR)

This instruction transfers the characters stored in 120 consecutive HSM locations to the Model 1033 Line Printer, causing one line to be printed. The operation can be obeyed in the Normal Mode when a prior instruction is being obeyed in the Simultaneous Mode. The Print Hold Off (PHO) button on the console will inhibit this facility.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

03: Paper Advance (PA)

This instruction positions the paper in the Model 1033 Line Printer for the next line of printing. It can advance the paper a specified number of lines, designated by $A_2A_3$, or by the punches in a tape loop on the Printer. This is a potentially simultaneous instruction. While in the Simultaneous Mode, it does not restrict the use of any other instruction in the Normal Mode except another PRINT (02) or PAPER ADVANCE (03) instruction.

04:*** Linear Read Reverse (LRR)

This instruction transfers one message from magnetic or paper tape to the HSM. It is a potentially simultaneous instruction. Though the tape is read in reverse, the characters will be placed in the HSM in their proper relative positions. LRR is most useful in sort routines since it saves rewind time.

05:*** Block Read Reverse (BRR)

This instruction transfers a block of characters from magnetic or punched paper tape into the HSM. Transfer begins with the first character following a gap and ends when the next gap is sensed. Though the tape moves in reverse, the characters will be placed in the HSM in their proper relative positions. The instruction is potentially simultaneous.

06:*** Unwind n Symbols (UNS)

This instruction causes a selected magnetic tape to be moved forward until a specified number of a designated symbol have been counted. The HSM is not altered. The instruction is potentially simultaneous, but no 'read' instruction can be executed simultaneously with it.

10:*** Transcribing Card Punch Write (TCW)

This instruction is the same as LINEAR WRITE (12) except that characters are written to tape at 12,500 char./sec.

N.B. Although the Transcribing Card Punch is no longer available, and the instruction is therefore redundant, it will nevertheless function correctly, in accordance with the manual, if used in error.

11:* Single Sector Write (SSW)

This instruction writes on to magnetic tape (or the Monitor Printer), and to the 1040 on-line printer, the contents of a sector located in any area of the HSM. This instruction can be executed only in the Normal Mode. However, a prior 'read' may, at the same time, be in the Simultaneous Mode.

12:*** Linear Write (LW)

This instruction transfers one message from the HSM to magnetic tape, the 1040 on-line printer, the Monitor Printer or to paper tape via the Monitor Printer. It is a potentially simultaneous instruction.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

13:* Multiple Sector Write (MSW)

This instruction writes on to magnetic tape, (or the On-Line and Monitor Printers), a single block comprising the contents of any number of sectors taken from various parts of the HSM under the direction of a stored list of addresses. This instruction is executed only in the Normal Mode, but a prior 'read' may, at the same time, be in the Simultaneous Mode.

14:*** Linear Read Forward (LRF)

This instruction brings one full message from magnetic or punched paper tape into the HSM. It is a potentially simultaneous instruction.

15:*** Block Read Forward (BRF)

This instruction brings a block of characters from magnetic or punched paper tape into the HSM. Transfer from tape begins with the first character following a gap, and ends when the next gap is sensed. This instruction is potentially simultaneous.

16:*** Rewind n Symbols (RNS)

This instruction causes a selected magnetic tape to be moved backwards through a specified number of symbols. This instruction is potentially simultaneous, but no 'read' instruction can be executed simultaneously with it. The HSM is not altered.

17: Rewind to BTC (RWD)

This instruction causes a designated magnetic tape to be completely rewound. Once the operation has been initiated, the rewind proceeds independently of the Computer, occupying neither the Normal nor the Simultaneous modes. The computer, after initiating the rewind, is free to execute other instructions.

21: Item Transfer (IT)

This instruction transfers an item from one group of successive HSM locations to another.

22: One-Character Transfer (OCT)

This instruction transfers the contents of one HSM location into another HSM location. It may be used to modify portions of instructions, transfer one-character constants, etc.

24: Sector Transfer by Character (STC)

This instruction transfers a series of characters from an area (sector) between, and including, two designated HSM locations to another HSM area (sector).

25: Three-Character Transfer (TCT)

This instruction transfers, in parallel, the contents of the three right-most locations of one tetrad to the corresponding locations of another tetrad in the HSM. It is useful for placing addresses into stored instructions, setting Address Modifiers, etc.

3. KDF 8 Supplement to the KDF 10 Programming Manual (Cont.) 3.

Sector Transfer by Tetrad (STT)

26: This instruction transfers the contents of one tetrad or any number of consecutive HSM tetrads between, and including, two specified tetrad addresses, into another specified tetrad or consecutive series of tetrads. This instruction differs from Sector Transfer by Character (24) in that it transfers four characters at a time, and is, therefore, four times faster.

27: Random Distribute (RD)

This instruction distributes successive items in the HSM, to locations designated by a stored list of addresses.

31: Locate $n^{th}$ Symbol in Sector (LNS)

This instruction searches through the contents of successive HSM locations between, and including, two given addresses, counting the occurrences of a designated symbol. The operation ceases when (1) the specified count is reached or (2) the right-most location in the sector has been searched.

32: Zero Suppress (ZS)

This instruction is used to delete the non-significant zeros to the left of the MSC of the result of a decimal arithmetic operation.

33: Justify Right (JR)

This instruction, used to effect right columnar alignment, (a) adjusts and transfers an item from one series of successive HSM locations to another, or (b) adjusts the item, leaving it in the same group of HSM locations. All the space symbols which were originally located to the right of the sign position are placed between the ISS and the MSD in the destination area. (The sign position is the HSM location immediately to the right of the LSD).

34: Sector Clear by Character (SCC)

This instruction places space characters in all the locations between, and including, two HSM addresses.

35: Sector Compress - Retain Redundant ISS's (SCR)

This instruction transfers a sector of characters from one part of the HSM to another, removing, in the process, all spaces located to the right of the rightmost non-space character within each item in the sector.

NOTE: A space in the sign position (i.e., positive sign) is also deleted.

36: Sector Clear by Tetrad (SCT)

This instruction inserts spaces $(01)_8$ in the HSM locations between, and including, two given tetrad addresses. It differs from the Sector Clear by Character Instruction (34) in that it clears four characters at a time, and is, therefore, four times faster.

37: Sector Compress - Delete Redundant ISS's (SCD)

This instruction transfers a sector of data from one part of the HSM to another, deleting, in the process, (a), all ISS's originally located to the

right of the rightmost non-ISS, non-space character in the sector, and (b), all spaces located to the right of the rightmost non-space character within each item in the sector.

NOTE: A space in the sign position (i.e., positive sign) is also deleted.

41: Binary Add (BA)

This instruction performs binary addition of two equal length operands and places the sum in the HSM locations originally occupied by the augend. The operands may be of any length. Each character (including control symbols) is treated as if it were numeric.

42: Binary Subtract (BS)

This instruction performs binary subtraction of one operand from another operand of equal length, placing the difference in the HSM locations originally occupied by the minuend. The operands may be of any length. Each character (including control symbols) is treated as if it were numeric.

43:* Sector Compare (SC)

This instruction is used to determine the relative magnitude of two operands of equal length. A single operand may consist of one character or any number of alpha-numeric characters and/or symbols. Binary subtraction is performed, but the difference is not stored in the HSM. However, the resultant PRI settings permit alternative sequences of instructions, to be chosen.

44:* Three-characters Add (TCA)

TCA is designed mainly to modify addresses of instructions and to keep octal counters. As such, it performs binary addition of an augend stored in the rightmost three locations of a tetrad and a three-character addend. The result is automatically stored in the locations previously occupied by the augend.

45:* Three-character Subtract (TCS)

Like the Three-Character Add, TCS is designed mainly for address modification and octal counters. It performs binary subtraction of two operands stored in the rightmost three locations of their respective tetrads. The difference is automatically stored in the locations previously occupied by the minuend.

46: Logical 'OR' (LO)

This instruction performs a function similar to the 'or' in machine logic, inserting '1' bits from a specified modifier into a specified operand of equal length.

47: Logical 'AND' (LA)

This instruction performs a function similar to the 'and' in machine logic. It may be used to extract '1' bits from an operand according to a second operand ('mask') of equal length.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

51: Decimal Add (DA)

This instruction performs decimal addition, in accordance with algebraic rules, producing a non-zero-suppressed sum, which is stored in the HSM locations originally occupied by the augend. The operands may be of any length and, also, of unequal lengths.

52: Decimal Subtract (DS)

This instruction performs decimal subtraction on variable length operands. The subtraction is algebraic. Specifications as to operands, storage of the difference and end conditions are exactly the same as in Decimal Add.

53: Decimal Multiply (DM)

This instruction performs decimal multiplication in accordance with algebraic rules, producing a non-zero-suppressed product. If a quantity is pre-stored in the product area, the product is added (absolute addition) to it, permitting round-off by any number and multiply-accumulate. However, the sign of the product will be assigned to the accumulated (absolute) result.

54: Decimal Divide (DD)

This instruction performs decimal division in accordance with algebraic rules and produces a non-zero-suppressed quotient. The non-zero-suppressed remainder is stored in the HSM locations originally occupied by the dividend. Each operand must carry a sign. The operands may be of any length. The length of each operand is defined by the first space to the left of a non-space, non-minus character, or by an ISS. If the divisor contains more digits than the dividend, the quotient will be a zero. Unlike the product in Decimal Multiply, the quotient is not added to a prestored quantity.

60:** Sense Simultaneous Operations

This instruction selects one of three sequences, depending on whether (a) Simultaneous Read mode (SIM01) and Simultaneous Write Mode (SIM02) are both occupied (b) only one of the simultaneous modes is occupied, or (c) both simultaneous modes are unoccupied.

61: Conditional Transfer of Control (CTC)

This instruction chooses one of three sequences of instructions, in accordance with the setting of the PRI's.

62:* Sense Simultaneous Mode (SSM)

This instruction chooses one of four sequences of instructions, depending upon whether the Simultaneous Modes are (a) unoccupied, (b) occupied by a 'read' instruction, or (c) occupied by a 'write' instruction, or (d) occupied by a paper advance (1033 printer only).

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

63:* Trunk Sense (TS)

This instruction tests the status of a given Tape Unit or on-line Model 1040 Printer, permitting program direction to one of two sequences of instructions.

64:* Sense Simultaneous Gate 2 (SSG2)

This instruction chooses one of two sequences of instructions depending on whether or not the Simultaneous Gate 2 is open.

65:* Sense Simultaneous Gate 1 (SSG1)

This instruction chooses one of two sequences of instructions, depending upon whether or not the Simultaneous Gate 1 is open.

66: Tally (TA)

This instruction permits looping through a sequence of operations by automatically reducing a pre-stored quantity each time control is transferred to the beginning of the sequence. When the quantity has been exhausted, the Tally ends and the instruction following it is performed.

71: Transfer Control (TC)

This instruction either causes an unconditional break in the sequence of instructions or takes action according to the settings of the Breakpoint Switches on the Computer Console.

72: Set Register (SET)

This instruction either replaces the contents of a specified register with the A address of the instruction, or sets a PRI.

73:* Store Register (STR)

This instruction places the contents of a selected register (or PRI setting) into the rightmost three locations of a designated tetrad.

74:** Control Simultaneous Gates 1 and 2 (CSG 1 & 2)

This instruction opens or closes the simultaneous gate to control two or three way simultaneity.

75:* Control Simultaneous Gate 1 (CSG 1)

This instruction is used to open or close the gate which controls entrance into the First Simultaneous Mode, making it possible to either prevent or permit simultaneous operations.

76: Stop (ST)

This instruction inhibits the staticising of any further instructions, halting the Computer after completion of any instruction in the Simultaneous Mode.

77: Return After Interrupt (RAI)

This instruction is used to re-enter a program after an unscheduled interruption, such as for Rollback or for a higher priority program.

The RAI was designed not only to transfer control, but also to permit both the A and B Registers to be properly set in the process. Thus, when the main program is re-entered, all of the pertinent conditions prevailing at the time of interruption can be re-established.

## 3.5 DETAILED DEFINITION AND DESCRIPTION OF NEW OR REVISED INSTRUCTIONS.

New instructions, or revised KDP 10 instructions, for KDF 8 are as follows:-

43 SECTOR COMPARE.
44 THREE CHARACTER ADD.
45 THREE CHARACTER SUBTRACT.
60 SENSE SIMULTANEOUS OPERATIONS.
62 SENSE SIMULTANEOUS MODE.
63 TRUNK SENSE.
64 SENSE SIMULTANEOUS GATE 2.
65 SENSE SIMULTANEOUS GATE 1.
73 STORE REGISTER.
74 CONTROL SIMULTANEOUS GATES 1 AND 2.
75 CONTROL SIMULTANEOUS GATE 1.

A full description of each of the above instructions is given in the following pages.

### 3.5.1 43.SECTOR COMPARE - SC.

General Description

This instruction is used to determine the relative magnitude of two operands of equal length. A single operand may consist of one character or any number of alpha-numeric characters and/or symbols. Binary subtraction is performed, but the difference is not stored in the HSM. However, the resultant PRI settings permit alternative sequences of instructions to be executed.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

Format

T register (preset)

Address of right-most character of the subtrahend.

A address:

Address of the left-most character of the minuend.

B address:

Address of the right-most character of the minuend.

Direction of Operation

Left to right or right to left.

Terminal Condition

The operation terminates when inequality is discovered, or when the right-most characters in the sectors have been compared. PRP will be set if the result is positive, PRZ if the result is zero, and PRN if the result is negative.

Final Register Contents

The A register store addresses the left-most character of the minuend. The B register addresses the first character to the left of the minuend. The T register addresses the first character to the left of the subtrahend.

N.B. If left to right compare $(B)_f = (A)_i$, but is converted to $(A)_i - (01)_8$ when carrying out a following STR B instruction.

Timing

(a) Operands are one character in length: 37.5 μs

(b) A or T Addresses refer to STA Tetrad: 37.5n μs
where n = numbers of characters in minuend.

(c) Operands are greater than one character and do not reference
STA: 37.5n
where n = no. of characters actually compared.

Outline of Logic

The A and T addresses are examined. If either directly references the STA tetrad, the instruction will operate from right to left. If the addresses do not reference the STA tetrad, STA will be simulated by transferring the contents of the A address to STA.

The A and B addresses are tested for equality. If they are equal, the instruction will operate from right to left. If the operands are greater than one character in length and the A and T addresses do not reference the STA tetrad, the following will occur:

The T Register will be adjusted to address the most significant (left-most) character of the subtrahend.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

The contents of the A and B Registers will be reversed so that the original contents of A are incremented, and the original contents of B remain static.

The instruction will terminate when operand inequality is recognised.

A positive result sets PRP, a negative result sets PRN, and a zero result sets PRZ.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

3.5.2 44. THREE CHARACTER ADD - TCA

General Description

TCA is designed to modify addresses of instructions and to keep octal counters. It performs binary addition of an augend stored in the right-most three locations of a tetrad and a three-character addend. The result is automatically stored in the locations previously occupied by the augend.

Format

| A address: | B address: |
|---|---|
| Address of right-most character of the augend (and sum). | Address of right-most character of the addend. |

Direction of Operation

Right to left.

Terminal Condition

The operation terminates when $C_1$ character of the augend has been replaced by the sum.

Final Register Contents

The A register store addresses the first character to the left of the sum. The B register addresses the first character to the left of the addend. The T register and P register store are unaffected.

Timing

Time in microseconds = 37.5 if both A and B address a $C_3$ position
otherwise = 37.5n

where n = 1 if A addresses a $C_1$ position
= 2 " $C_2$ "
= 3 " $C_3$ "
= 4 " $C_0$ "

Outline of Logic

The TCA instruction operates according to the following rules:

1. There is no search for the least significant characters or signs of the operands. Every character enters into addition.

2. The PRI's are not affected by the TCA, and a sign is not stored in the sum.

3. The addition considers all six bits of the characters in the operands.

4. Any carry from the most significant bit position of the sum is discarded.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

5. All characters are treated as numeric; there are no special control symbols. The addition ends when the two least significant bits in the A register are 01. (Note that, although this termination condition is constant, addition actually starts with the characters in the locations designated by the A and B addresses. TCA can, therefore also be used as a one or two-character add if the A address refers to $C_1$ or $C_2$ of a tetrad, or as a four-character add if the A address refers to $C_0$ of the tetrad to the right. If, however, addition starts with the $C_3$ character of both Augend and Addend, the addition is carried out on all three characters in parallel. This is also applicable to the Three-Character Subtract instruction).

6. The sum replaces the augend in the HSM, character for character.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

3.5.3 45. THREE CHARACTER SUBTRACT - TCS

General Description

Like Three-Character Add, TCS is designed for address modification and octal counters. It performs binary subtraction of a minuend stored in the right-most three locations of a tetrad and a three-character subtrahend. The difference is stored in the locations previously occupied by the minuend.

Format

| A address: | B address: |
|---|---|
| Address of right-most character of the minuend (and difference). | Address of right-most character of the subtrahend. |

Direction of Operation

Right to Left.

Terminal Condition

The operation terminates when $C_1$ character of the minuend has been replaced by the difference.

Final Register Contents

The A register store addresses the first character to the left of the difference. The B register addresses the first character to the left of the subtrahend. The T register and P register store are unaffected.

Timing

Time in microseconds = 37.5 if both A and B address a $C_3$ position.
otherwise = 37.5n

when n = 1 if A addresses a $C_1$ position
= 2 " $C_2$ "
= 3 " $C_3$ "
= 4 " $C_0$ "

Outline of Logic

The TCS instruction operates according to the following rules:

1. Every character enters into the subtraction. There is no search for the signs or least significant characters of operands and there are no special control symbols. The operation ends when the two least significant bits in the A register are 01.

2. A sign is not stored to the right of the difference, although the PRI's are properly set to reflect the relative magnitudes of the operands.

3. The subtraction considers all six bits of characters in the operands.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

4. The subtrahend is complemented ('ones' complement) and a binary addition is performed.

5. A '1' (complementary carry) is automatically added into the least significant bit position of the difference. Any carry from the most significant position is discarded. If there was a carry, the difference is positive; if no carry, the difference is negative.

6. The difference replaces the minuend in the HSM.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.)

3.5.4 60. SENSE SIMULTANEOUS OPERATIONS - SSO

General Description

This instruction selects one of three sequences, depending upon whether (a) Simultaneous Read Mode (SIMO I) and Simultaneous Write Mode (SIMO II) are both occupied, (b) only one of the simultaneous modes is occupied, or (c) both simultaneous modes are unoccupied.

Format

A address:

HSM location of the next instruction to be executed if both simultaneous modes are occupied.

B address:

HSM location of the next instruction to be executed if one simultaneous mode is occupied.

If both simultaneous modes are unoccupied, the instruction in the location immediately following the SSO instruction is executed.

Outline of Logic

A test is made of the simultaneous mode indicators. If not set, the SSO ends and the computer continues to the next instruction in sequence. If both simultaneous indicators are set, the contents of the P Register are stored in standard HSM locations and the contents of the A Register are transferred to the P Register. If only one simultaneous indicator is set the contents of the P Register are stored in standard HSM locations and the contents of the B Register are transferred to the P Register.

NOTE: STA is not performed in this instruction.

Final Register Contents

$(A)_f = (A)_i$
$(B)_f = (B)_i$

Timing.

$12\frac{1}{2}$ µs.

3. KDF 8 Supplement to the KDP 10 programming Manual (Cont.)

3.5.5 62. SENSE SIMULTANEOUS MODE - SSM

General Description

This instruction selects on of four sequences of instructions depending upon whether (a) the Simultaneous Modes are unoccupied, (b) the Simultaneous Read Mode (SIMO I) is occupied by a read instruction (c) the Simultaneous Write Mode (SIMO II) is occupied by a write instruction, (d) the Simultaneous Read Mode (SIMO I) is occupied by a Paper Advance (1033 printer only).

Format

A address:

HSM location of next instruction to be executed if a read is in the Simultaneous Read Mode (SIMO I).

B address:

HSM location of the next instruction to be executed if a write is in Simultaneous Write Mode (SIMO II).

If both Simultaneous Modes are unoccupied, the instruction in the location immediately following the SSM instruction is executed.

If both Simultaneous Modes are occupied, the instruction is held off until one mode becomes free.

If a Paper Advance instruction (03) is in SIMO I control is automatically transferred to HSM location (000200).

Outline of Logic

A test is made of the Simultaneous Mode indicators. If neither is set, the SSM ends and the computer continues to the next instruction in sequence. If either is set, the contents of the P Register are stored in standard HSM locations and the read, write, and paper advance indicators are tested, in accordance with which the address of the next instruction to be executed is placed in the P Register.

NOTE: STA is not performed in this instruction.

Registers Used

A B

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

$12\frac{1}{2}$ µs.

### 3.5.6 63. TRUNK SENSE - TS

General Description

This instruction tests the status of a given Tape Unit or On-line Printer (Model 1040) permitting program direction to one of two sequences of instructions.

Format

A address:

Address of the next instruction to be executed if the condition or one of the conditions being tested is present.

B address:

Where $B_1$ = Tape Unit number

$B_2$ = Tests to be performed. (111111) in $B_2$ will perform all six tests; (000001) will perform only the first test.

| '1' Bit In | Test |
|---|---|
| $2^0$ | Is the tape positioned on BTC? |
| $2^1$ | Has ETW been sensed? |
| $2^2$ | Is the tape now stationary or moving forward? |
| $2^3$ | Is the tape now moving in a reverse direction? |
| $2^4$ | Is the tape now in motion? |
| $2^5$ | Is the tape unit non-operable? |

$B_3$ = Not used.

Where $B_1$ = On-line Printer number.

$B_2$ = The following tests:

| '1' Bit In | Test |
|---|---|
| $2^0$ | Is the printer ready? (i.e., finished printing). |
| $2^1$ | No significance. |

| '1' Bit In | Test |
|---|---|
| $2^2$ | Is the printer ready to receive more data, or is the computer still transferring data? |
| $2^3$ | Is the printer printing? |
| $2^4$ | Is the computer transferring data? |
| $2^5$ | Is the printer inoperable? |

$B_3$ = Not used.

If the $B_1$ character is $(77)_8$ and the SR register is occupied the Monitor Printer will be tested; if the $B_1$ character is $(77)_8$ and the SR register is unoccupied the Paper Tape Reader will be tested. In either case, the only valid test would be with respect to operability (1 bit in $2^5$).

Final Register Contents

The A register store is unaffected. The B register contains the B address of the instruction modified by $N_B$. If the condition or one of the conditions being tested is present, the P register contains the A address of the instruction modified by $N_A$ and the P register store addresses the instruction in the location immediately following the TS. If the condition or conditions are not present, the P register addresses the instruction in the location immediately following the TS and the P register store is unaltered. The T register is unaltered.

Timing

25 μs if no transfer of control )
37.5 μs if a transfer is executed ) + $12\frac{1}{2}$ μs if both simultaneous modes were previously occupied, plus Hold Off Time.

Outline of Logic

The instruction is held off if both simultaneous modes are occupied, until one of them becomes unoccupied, so that it may then use the SW or SR registers.

The Tape Unit number ($B_1$) is placed in either the SW or the SR register (whichever is unoccupied). The tests called for by the '1' bits in $B_2$ are performed. If any one of the conditions tested is present, the contents of the P register are transferred to standard HSM locations and the contents of the A register are then transferred to the P register, effecting transfer of control to the instruction specified by the A register. If a transfer is not called for, the next instruction in sequence will be executed. The TS instruction does not go through STA.

### 3.5.7 64. SENSE SIMULTANEOUS GATE 2 - SSG2

General Description

This instruction chooses one of two sequences of instructions depending upon whether or not the Simultaneous Gate 2 is open.

Format

A address:

HSM location of the next instruction to be executed if Simultaneous Gate 2 is open.

B address:

HSM location of the next instruction to be executed if Simultaneous Gate 2 is closed.

Outline of Logic

The contents of the P Register are stored in standard HSM locations (STP). The gate controlling entrance to SIMO II is examined. If it is closed, the contents of the B Register are transferred to the P Register. If the gate is open, the contents of the A Register are transferred to the P Register.

NOTE: STA is not performed by this instruction.

Addressable Registers Used

A B

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

$12\frac{1}{2}$ µs.

### 3.5.8 65. SENSE SIMULTANEOUS GATE 1 - SSG1

General Description

This instruction chooses one of two sequences of instructions, depending upon whether or not the Simultaneous Gate 1 is open.

Format

A address:

HSM location of the next instruction to be executed if Simultaneous Gate 1 is open.

B address:

HSM location of the next instruction to be executed if Simultaneous Gate 1 is closed.

Outline of Logic

The contents of the P Register are stored in standard HSM locations (STP). The gate controlling entrance to SIMO I is examined. If it is closed, the contents of the B Register are transferred to the P Register. If the gate is open, the contents of the A Register are transferred to the P Register.

NOTE: STA is not performed by this instruction.

Addressable Registers Used

A B

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

$12\frac{1}{2}$ µs.

3.5.9 73. STORE REGISTER - STR

General Description

This instruction places the contents of a selected register into the right-most three locations of a designated tetrad.

Format

A address:

Specifies the tetrad that is to receive the contents of the designated register.

B address:

Specifies the PRI's or the register whose contents are to be stored.

| $B_1$ Character | Register Selected |
|---|---|
| $(10)_8$ | PRI's |
| $(20)_8$ | $S_1$ Register |
| $(30)_8$ | B Register |
| $(40)_8$ | P Register |
| $(50)_8$ | $S_1$ Register if Simultaneous Read Mode. (SIMO I) last activated. $S_2$ Register if Simultaneous Write Mode. (SIMO II) last activated. |
| $(60)_8$ | T Register |
| $(70)_8$ | $S_2$ Register |

$B_2$ $B_3$ - Ignored.

Outline of Logic

The $B_1$ character is examined in the SC Register. The contents of the designated register are then stored in $C_1$, $C_2$, $C_3$ of the tetrad specified by the A address; the original $C_0$ remains undisturbed.

If the $B_1$ character in an STR instruction is $(10)_8$ the value that will be stored in the tetrad specified by the A address will be $(000001)_8$ if PRN is set, $(000002)_8$ if PRZ is set, and $(000004)_8$ if PRP is set.

If $B_1$ is $(50)_8$, the $S_1$ Register is stored if a read was last activated; if a write was last activiated, the $S_2$ Register is stored.

If the $B_1$ character is not one of the values listed (Format), the instruction will not be executed, but the timing will be the same as if it had been executed. No alarm stop will occur. The program will continue to the next instruction in sequence. (Note that the A Register is not included in the list). This instruction does not go through STA.

If SC = 30 and the instruction follows a sector compare instruction, then (B-1) is stored. This corrects the fact that with Sector Compare (left to right), the final address left in B was one greater than it ought to be.

Addressable Registers Used

A Register specified.

Final Register Contents

Normally $(A)_f = (A)_i - (01)_8$

$(B)_f = (B)_i$

But when this instruction follows a Sector Compare and B1 = 30 then

$(A)_f = (A)_i$

Timing

$12\frac{1}{2}$ vs.

3. KDF 8 Supplement to the KDP 10 Programming Manual (Cont.) 3.

3.5.10 74. CONTROL SIMULTANEOUS GATES 1 AND 2 - CSG (1 & 2)

General Description

This instruction opens or closes the simultaneous gates to control two or three way simultaneity.

Format

A address:

Ignored.

B address:

$B_1 - 2^0$

If 0, simultaneous gate 1 is to be opened.

If 1, simultaneous gate 1 is to be closed.

$B_1 - 2^1$

If 0 simultaneous gate 2 is to be opened.

If 1 simultaneous gate 2 is to be closed.

$B_2$ $B_3$ - ignored.

NOTE: This instruction does not go through STA.

Addressable Registers Used

B

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

$12\frac{1}{2}$ us.

3.5.11 75. CONTROL SIMULTANEOUS GATE 1 - CSG 1.

General Description

This instruction will open or close the gate which controls two way simultaneity, making it possible either to prevent or to permit simultaneous operations.

Format

A address:

Ignored.

B address:

$B_1$ - must be even ($2^0$ bit = '0') if gate 1 is to be opened, and
odd ($2^0$ bit = '1') if gate 1 is to be closed.

$B_2B_3$ - ignored.

NOTE: This instruction does not go through STA.

Addressable Registers Used

B

Final Register Contents

$(A)_f = (A)_i$

$(B)_f = (B)_i$

Timing

12½ µs.

## 4. KDF 8 INSTRUCTION TIMING (EXCLUDING TAPE HANDLING FUNCTIONS) 4.

The timing formulae do not include staticising, automatic address modification, or STA time. To obtain the overall timing, the following items should be added where appropriate:

a) Staticising time of 25 μs (Constant for each instruction.)

b) Automatic address modification time of 25 μs if either the A or the B address is to be modified; or 50 μs if both addresses are modified.

c) STA time of 12.5 μs.

* The timing formula given for "Random Distribute" (27) is a weighted average;

| OP CODE | INSTR$^{N.}$ | TIMING IN MICROSECONDS | STA? | NOTES |
|---|---|---|---|---|
| 01 | PES | STATICISING TIME | YES | |
| 21 | IT | 25n | YES | n = No. of characters transferred |
| 22 | OCT | 25 | YES | |
| 24 | STC | 25n | YES | n = No. of characters transferred |
| 25 | TCT | 25 | YES | |
| 26 | STT | 25n | YES | n = No. of tetrads transferred |
| 27 | RD * | $27.5n_1+15n_2+37.5n_3$ | YES | $n_1$= Total no. of characters transferred<br>$n_2$= Total no. of characters whose distribution address is $(777777)_8$<br>$n_3$= No. of distribution addresses left when 'EM' is found (the address of 'EM' must be included in $n_3$) |

4. KDF 8 Instruction Timing (Cont.) 4.

| OP CODE | INSTR$^{N.}$ | TIMING IN MICROSECONDS | STA? | NOTES |
|---|---|---|---|---|
| 31 | LNS | 12.5m + 25n + 37.5<br>12.5 if count zero<br>50 if sector is one character in length | YES | n = No. of occurances counted<br>m = Total no. of locations searched |
| 32 | ZS | a. 12.5m+25n+12.5<br>b. 12.5m+25n<br>c. 25 | YES | a. In usual case<br>b. If ZS terminated by A-B equality<br>c. If no zeros or spaces found<br>m = No. of spaces preceding first none-space character<br>n = No. of zeros suppressed |
| 33 | JR | 25n + 25m | YES | n = No. of space and/or minus characters to the rightmost non-minus, non-space character<br>m = No. of non-space, non-minus characters (including ISS) transferred |
| 34 | SCC | 12.5n | YES | n = Total no. of locations cleared |
| 35 | SCR | 12.5n + 12.5m | YES | n = Total no. of characters actually transferred<br>m = Total no. of characters in original sector |
| 36 | SCT | 12.5n | YES | n = Total no. of tetrads cleared |
| 37 | SCD | 12.5n + 12.5m | YES | n = Total no. of characters actually transferred<br>m = Total no. of characters in original sector |
| 41 | BA | 37.5n | YES | n = No. of characters in augend |

4. KDF 8 Instruction Timing (Cont.) 4.

| OP CODE | INSTR$^{N.}$ | TIMING IN MICROSECONDS | STA? | NOTES |
|---|---|---|---|---|
| 42 | BS | 37.5n | YES | n = No. of characters in minuend |
| 43 | SC | a. 37.5<br>b. 37.5n<br>c. 37.5m + 37.5 | YES | a. Operands one character in length<br>b. 'A' or 'T' addresses reference STA tetrad.<br>n = No. of charaters in minuend<br>c. Operands are greater than one character and do not reference STA.<br>m = No. of characters actually compared |
| 44 | TCA | a. 37.5<br>b. 37.5n | YES | a. Three character operands<br>b. 1, 2, or 4 character operands<br>n = 1, 2, or 4 |
| 45 | TCS | a. 37.5<br>b. 37.5n | YES | a. Three character operands<br>b. 1, 2, or 4 character operands<br>n = 1, 2, or 4 |
| 46 | LO | 37.5n | YES | n = No. of characters in operand to be modified |
| 47 | LA | 37.5n | YES | n = No. of characters in operand to be modified |
| 51 | DA | $12.5n_1+37.5n_2+25n_3+75$ | YES | $n_1$= Total no. of space and/or minus characters found to the right of both operands<br>$n_2$= No. of digits in shorter operand<br>$n_3$= Difference in no. of digits of the two operands<br>If result is negative and the sum is re-complemented add 25(n+1)+12.5 where n = No. of digits in the result |

4. KDF 8 Instruction Timing (Cont.) 4.

| OP CODE | INSTR^N. | TIMING IN MICROSECONDS | STA? | NOTES |
|---|---|---|---|---|
| 52 | DS | SAME AS DECIMAL ADD | YES | |
| 53 | DM | a. $n_1 > 0$, $n_2 > 0$<br>$12.5\left[10+(12n_1+32)n_2\right] + 12.5n_3$<br>b. $n_1 = 0$, $n_2$ 0<br>$12.5(n_2+n_3+3)$<br>c. $n_2 = 0$, $n_1 > 0$<br>$12.5(n_1+n_3+3)$<br>d. $n_1 = n_2 = 0$ | YES | $n_1$= No. of digits in multiplicand<br>$n_2$= No. of digits in multiplier<br>$n_3$= Total no. of spaces (including sign) and/or minuses to the right of LSD's of operands |
| 54 | DD | a. $n_1 \geq n_2$<br>$12.5\left[26n_1-7n_2+12.5n_2 (n_1-n_2)+41\right] +12.5n_3$<br>b. $n_1 < n_2$<br>$12.5(3n_1+n_2+12)+ 12.5n_3$<br>c. $n_1 = 0$ (dividend missing, ie. an ISS alone or all spaces and an ISS)<br>$12.5(n_2+7)+12.5n_3$ | YES | $n_1$= No. of digits in dividend<br>$n_2$= No. of digits in divisor<br>$n_3$= Total no. of spaces (including sign) and/or minuses to the right of LSD's of operands |
| 60 | SSO | 12.5 | NO | |
| 61 | CTC | a. Staticising time only<br>b. 12.5 | NO | a. if zero path taken<br>b. if plus or minus path taken |
| 62 | SSM | 12.5 | NO | |
| 63 | TS | a. 25<br>b. 37.5 | NO | a. if no transfer of control<br>b. if transfer executed |

4. KDF 8 Instruction Timing (Cont.) 4.

| OP CODE | INSTR$^{N.}$ | TIMING IN MICROSECONDS | STA? | NOTES |
|---|---|---|---|---|
| 64 | SSG 2 | 12.5 | NO | |
| 65 | SSG 1 | 12.5 | NO | |
| 66 | TA | a. 25<br>b. 37.5 | NO | a. If quantity tested is $(000000)_8$<br>b. If quantity greater than $(000000)_8$ |
| 71 | TC | 12.5 | NO | |
| 72 | SET | 12.5 | - | STA only if 'A' register set |
| 73 | STR | 12.5 | NO | |
| 74 | CSG1&2 | 12.5 | NO | |
| 75 | CSG1 | 12.5 | NO | |
| 76 | ST | STATICISING TIME | YES | |
| 77 | RAI | 12.5 | YES | |

5. KDP 10 AND KDF 8 CHARACTER CODE 5.

| OCTAL EQUIV. | CHARACTER DESCRIPTION | SYMBOL | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Channel Number | | | | | |
| | | | p | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | | | | BIT VALUE | | | | | |
| 00 | Blank | | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 01 | Space | - | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 02 | Cross | ≠ | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 03 | Open Parenthesis | ( | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 04 | Close Parenthesis | ) | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 05 | Quotes | " | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 06 | Colon | : | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 07 | Pound sterling | £ | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 10 | Per cent | % | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 11 | Semicolon | ; | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 12 | Ampersand | & | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 13 | Apostrophe | ' | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 14 | Minus | - | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 15 | Asterisk | * | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 16 | Full stop | . | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 17 | Carriage Shift (CS) | | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 20 | Page Change (PC) | | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 21 | Line Shift (LS) | | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 22 | Stroke | / | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 23 | Zero (Numeric) | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| 24 | One | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 25 | Two | 2 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 26 | Three | 3 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 27 | Four | 4 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 30 | Five | 5 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 31 | Six | 6 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 32 | Seven | 7 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| 33 | Eight | 8 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 34 | Nine | 9 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 35 | Comma | , | 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 36 | Number | # | 1 | 0 | 1 | 1 | 1 | 1 | 0 |
| 37 | Carriage Normal | | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 40 | A | A | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 41 | B | B | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 42 | C | C | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| 43 | D | D | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 44 | E | E | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 45 | F | F | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 46 | G | G | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 47 | H | H | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 50 | I | I | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 51 | J | J | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 52 | K | K | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 53 | L | L | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 54 | M | M | 0 | 1 | 0 | 1 | 1 | 0 | 0 |

| OCTAL EQUIV. | CHARACTER DESCRIPTION | SYMBOL | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Channel Number | | | | | |
| | | | p | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | | | | BIT VALUE | | | | | |
| 55 | N | N | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 56 | O | O | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 57 | P | P | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 60 | Q | Q | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 61 | R | R | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 62 | S | S | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 63 | T | T | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 64 | U | U | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 65 | V | V | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 66 | W | W | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 67 | X | X | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 70 | Y | Y | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 71 | Z | Z | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 72 | End File (EF) | | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 73 | End Data (ED) | | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 74 | Item Separator (ISS) | ° | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 75 | End Message (EM) | > | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 76 | Start Message (SM) | < | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 77 | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

NOTE: The octal values assigned to certain characters on the 1040 High-Speed Line Printer may be interchanged by means of a Code Plug. The character Code shown above is the Model 1033 and 1035 compatible set to which all Software is standardized.

# 6. ERROR CONDITIONS, CONSOLE INDICATORS, ROLLBACK, ETC. 6.

## 6.1 ERROR CONDITIONS

Normal Mode Error Stop - If an error occurs in the normal moade the normal mode operation will halt but both simultaneous operations (if in use) will run to completion before the computer halts. If, during this time, an error occurs in one of the simultaneous modes, the operation being performed in that mode will halt but the other simultaneous operation will run to completion before the computer halts.

Simultaneous Mode Error Stop - If an error occurs in one of the simultaneous Modes, the operation being performed in that mode will halt but the normal and other simultaneous operation will run to completion before the computer halts. If, during this time, an error occurs in either the normal or other simultaneous mode, the mode in which the error occurred will halt but the instruction in the other mode will run to completion before the computer halts.

Immediate Stop - If an immediate stop occurs the current status level will be completed and the computer will halt.

## 6.2 CONSOLE INDICATORS

ISIM - Inhibit Simultaneity.

This button, when depressed, causes all instructions to be performed serially but in the designated mode.

SMDI - Simultaneous Mode Inhibit.

This button, when depressed, causes all simultaneous instructions to be executed in the normal mode.

STCP - Simultaneous Transcribing Card Punch Write.

This indicator, when illuminated, indicates that a Transcribing Card Punch Write is going on.

SO 1

This is the present SO pushbutton indicator. When depressed, it opens Simultaneous Gate 1.

SO 2

This is a new pushbutton indicator. When depressed, it opens Simultaneous Gate 2.

SGR

This is the present SG pushbutton indicator which indicates that a simultaneous read or paper advance status level is going on.

SGW

This is a new pushbutton indicator which indicates that a Linear or a TCP write status level is going on.

6. Error Conditions, Console Indicators, Rollback, Etc. (Cont.) 6.

6.3 ROLLBACK

Hardware and software rollback will operate without modification.