EMAS 2900 HARDWARE NOTE

No: 1
Date: 17/2/78

Information on 2900 Image Store

(Received verbally by J.K. Yarwood from Alan Darling and Bill Kell, 4th May, 1977; updated June 1977; updated with the help of Pat Ryan January 1978.)

The purpose of the discussion was to establish differences between the 2980 and the 2976, 2970 & 2960 with a view to trying EMAS 2900 on the former. The following table summarises the model-dependent addresses and uses for the four machines:

	2960.Bits	SML16 2970.Bits	2976.Bits	SML12 2980.Bits
OCP Registers				
LST Base	00006001	00006001	402A	402A
LST Limit	6000	6000	402C	402C
PST Base	6003	6003	4029	4029
PST Limit	6002	6002	402B	402B
Handkeys	6006	6006	4205	4205
Hooter (set bit to commence hoot; clear bit to terminate hoot)	6008 31 (Optional)	6008 31	4013 19	4013 19
System Interrupt Register (Bit set to indicate interrupting Port)	600A 28-31 for Ports 0 to 3	600A 28-31 for Ports 0 to 3	4014 22-27 for Ports 0 to 5	4014 22-27 for Ports 0 to 5
Real time clock (X)	600C	600C	44pt4000	44pt4000
Real time clock (Y)	600D	600D	44pt4100	44pt4100
Real time clock (Z)	600E	600E	44pt4200 (see footnote)	44pt4200 (see footnote)

	2960.Bits	SML16 2970.Bits	2976.Bits	SML12 2980.Bits
OCP Control Registers				
Control (inhibit when set)	6011	6011	4013	4013
Clear slaves - write only (reads 0)	0			
Inhibit CPRs		24		
Inhibit main store		25		
Inhibit retry		26	13	13
Inhibit pipeline		27	12 (non overlap)	12 (non overlap
Inhibit stack slave		28	20	20
Inhibit instruction slave			23	23
Inhibit operand slave	28		28	28
Inhibit full photo	31			
Lock translation slave rejection			25	25
Software Gen. System Error	6013	6013	4013 17	4013 17
Register Load ('Activate')	6014	6014	not implemented	not implemented
SMAC Image Store				
SMAC config. register (one per SMAC) (s = SMAC ident no, in range 0-F)	4C0s6A20	4C0s6A20	4Cs04A20	4Cs04A20
Available blocks	8-23 bit 23=block 0,	8-23 bit 22=block 1,	8-23 bit 21=block 2, etc	7-22 bit 7=block 0, bit 8=block 1, etc
SMAC blocksize	128K /256	128K /256	128K	256K

9.9 29604

2970 SMAC IMAGE STORE MAP

I.S. ADDR	4CXX6004	4CXX6100	4CXX6A00	4CXX6A10	4CXX6A20
Data bit No.	Failing Data	Failing Address	Status	Engineering Status	Configuration
32	Hamming Parity 0	Address Parity		On Margins	0 BLK Conf as Ø
33	Hamming Parity 1			Inhibit Hamming Check	1 "
34	Hamming Parity 2			Inhibit Hamm. Report	2 "
35	Hamming Parity 3			On 'Engineers'	3 "
36	Hamming Parity 4	Address bit 04		Basic Unit Select	
37	Hamming Parity 5	Address bit 05		Add. Unit Select	
38	Hamming Parity 6	Address bit 06		Add. Unit Select	
39	Hamming Parity Word-	Address bit 07		Add. Unit Select	
40		Address bit 08	Port 0 Fail		Block 15 On line
41		Address bit 09	Port 1 Fail		Block 14 On Line
42		Address bit 10	Port 2 Fail		Block 13 On Line
43		Address bit 11	Port 3 Fail		Block 12 On Line
44		Address bit 12	Hamm. Gen. Fail		Block 11 On Line
45		Address bit 13	Hamm. Corr. Fail		Block 10 On Line
46		Address bit 14	I.S. NACK		Block 09 On Line
47		Address bit 15			Block 08 On Line
48	Byte 0 Parity Fail	Address bit 16	Byte Parity Fail		Block 07 On Line
49	Byte 1 Parity Fail	Address bit 17	Address Parity Fail		Block 06 On Line
50	Byte 2 Parity Fail	Address bit 18	Byte Func.Par.Fail		Block 05 On Line
51	Byte 3 Parity Fail	Address bit 19			Block 04 On Line
52	Byte 4 Parity Fail	Address bit 20			Block 03 On Line
53	Byte 5 Parity Fail	Address bit 21			Block 02 On Line
54	Byte 6 Parity Fail	Address bit 22			Block 01 On Line
55	Byte 7 Parity Fail	Address bit 23	Multibit Hamm. Fail		Block 00 On Line
56		Address bit 24	Singlebit Hamm. Fail	Marginate + 5v	Not Natural SMAC No.
57		Address bit 25	Reading Fault	Marginate - 5v	Be SMAC No. 1
58		Address bit 26	IPC 'X' Toggle Set	Marginate 19v	Port 0 Closed
59		Address bit 27	Holding Fault	Marginate 3.5v	Port 1 Closed
60		Address bit 28	Control Parity Fail	+5v Margins High	Port 2 Closed
61		Address bit 29	A.U.Addr.Par. Fail	-5v Margins High	Port 3 Closed
62				19v Margins High	BLK 1 in BU
63				3.5v Margins High	BLK Ø in BU

2960.Bits SML16 2970.Bits 2976.Bits SML12 2980.Bits

SAC Trunk Register Image Store (2980 only)

DATA IN (B->A)

SPAD contents (i.e. RAM) { 40pt4000 0-31; 4100 32-63; 4200 64-95; 4300 96-127

SAC Registers

These are all model-independent.

[Footnotes:

1) 2980 Real-time Clock

pt is where you get the IPL interrupt from: p is normally 0 and t is "don't care" (zero).

You must also set the appropriate port bit in 4012 (bits 16 to 25 = Ports 0 to 5) to allow SAC external interrupts to reach the OCP.

The Real-time clock on the 2980 is out in a (the) SAC.

The 2976 is as the 2980 but p' = OCP port.

2) 2960 Real Addressing Mode

This is now thought to be available.]

J.K. Yarwood
P.D. Stephens

Image store locations on P2; subblock 60

All locations are read/write unless otherwise specified (or reserved)

6000	-	LSTB0
6001	-	LSTB1
6002	-	PSTB0
6003	-	PSTB1
6004	-	Reserved
6005	-	Reserved
6006	-	Handkeys (read only)
6007	-	Machine type (read only)
6008	-	Hooter (read zero, write bit 2**0 to set/clear hoot)
6009	-	Broadcast system errors (bit 2**0) (read and write)
600A	-	System interrupt mask
600B	-	Communications SMAC number
600C	-	RTCX
600D	-	RTCY
600E	-	RTCZ
600F	-	Clock module number
6010	-	Reserved
6011	-	CPU mode and control
6012	-	Reserved
6013	-	Cause system error (read zero, write to bit 2**7)
6014	-	Block 0 activate (write only)
6015	-	Reserved
6016	-	Upper lights (write only)
6017	-	Lower lights (write only)
6018	-	Stop machine (write only)

R.D. Eager
17th August 1982

Details of image store X6011 on P2

Image store read

A read returns bits 2**15 to 2**0 of the OCP control register (working store X27).

Image store write

The effect of a write is controlled by bits 2**16 and 2**17 of the operand. The combined values of these two bits have the following effect:

00 => Bits 2**0 to 2**15 of operand replace corresponding bits in the control register
01 => Bits 2**0 to 2**15 of operand are 'or'd into the control register
10 => Bits 2**0 to 2**15 of operand are cleared in the control register
11 => Illegal; gives program error 9, subclass 4

Meaning of bits in control register

2**0 - Inhibit full photograph
2**1 - Inhibit photograph
2**2 - Not used
2**3 - Inhibit data slaves
2**4 - Not used
2**5 - Inhibit retries
2**6 - Not used
2**7 - Inhibit hamming correction reporting
2**8 - Not used
2**9 - Pull HELP on program error
2**10 - Stop on program error
2**11 - Not used
2**12 - Inhibit photo on soft system error
2**13 - Retry in progress
2**14 - Stop after photograph
2**15 - Error handling in progress

R.D. Eager
16th August 1982

EMAS 2900 HARDWARE NOTE

No: 2
Date: 15/12/77

ICL 2970 Engineer's Panels

The attached description of the 2970 Engineer's panels has been taken from two ICL technical documents (diagrams: 65/94562, text: 65/94563); it describes the current state of the panels, i.e. following the SML19 hardware upgrade.

The question of providing this information was raised originally by my receipt (via John Maddock) of a similar document produced by the Post Office, relating to the Barbican machine. A number of people using the 2970 expressed an interest in it. However, although the P.O. document contains a slightly fuller description of the handkeys and indicators than the attached note, it is now out of date as a result of SML19. Nonetheless, much of the information in it is still relevant to our 2970; I have kept it and can give anyone interested a listing. It has been filed as Hardware Note 2a.

I should like to thank Les Mowbray (ICL 2900 Engineer) and John Maddock for their help.

John M. Murison

1 GENERAL LAYOUT

The OCP Engineer's facilities comprise 19 rows of monitor lamps with 72 lamps in each row & 1 row of monitor lamps with 36 lamps and 3 rows of handkeys with 36 in each row. The layout of handkeys and monitor lamps are shown on OD61 to 64 of document 65/94562 and their operational usage is described in the following text.

2 MONITOR LAMPS (Brackets at row number indicate MDP socket)

Row 1 (1R) The group of seven lamps at the left-hand end of this row display ARU Fails; AK, LX, AL, AQ, XC, AN and MF. The remaining lights display the ARU K highway (bits 00-63).

Row 2 (2R) The ARU Parity Flags are indicated by the group of six lamps situated at the left hand end of this row; AK, LX, AL, AQ, ASE (Inhibit System Error), and FP (Force Parity error). The remaining lamps display the ARU L highway (bits 00-63).

Row 3 (3R) The ARU AA and AP parity stats. (E, A and L) are displayed at the left hand end of this row. The remaining lamps are devoted to displaying the ARU Q highway (bits 2-63).

Row 4 (4R) The ARU AS and RAM parity stats. (E, A and L) are displayed at the left hand end of this row, the remainder display the contents of the ARU Ram (00-63).

Row 5 (11R)

RIF	00 - 06	IFU
RIK	00 - 06	
RHF	00 - 06	
RHK	00 - 06	
IL	00,01	
ISL	27,28	PC
RIF	27 - 30	
RHF	27 - 30	
FI		Function Dependant Flags
FSK		
FTOS		
FD		AGU Microprogram Flags
FX	General Purpose Flags	
FY		
FZ		
FTS		
JAM	Real Address Mode	
D	PSR D bit see IM110 for fuller explanation	
PRIV	Privilege	
DGW	Diagnostic Write	
MK	E,A,L Parity Stats	
RMFP	ARU Mask and Filler Parity	
RMF	00 - 15 ARU Mask and Filler.	

Row 6 (12R)	RGF	00 - 06	AGU Function Register
	RGK	00 - 05	
	ROP	00, 14 - 31	
	IBE		Instruction Buffer empty.
	SUCJ		Jump condition satisfied.
	EP		Event pending
	RAN	P, 00 - 07	ARU AN register
	RAP	00 - 03, 62, 63	ARU AP bits
	RMK	30, 31, 62, 63	ARU MK bits
	MILLSH	OM, OL, 01-05	
	APSH	00-02	AP shift
	MK	$\overline{01}$, $\overline{02}$	
	AA	$\overline{01}$	
	RAG	P, 00-03	
Row 7 (13R)	PC	00-30	AGU PC
	BV		AGU B Overflow.
	CC	00,01	AGU CC
	GAZ	00,01	AGU ACC size.
	GOZ	00,01	AGU Operand size.
	GTWIST		AGU TWIST stat.
	RRF	00-07	Buffer Function Register.
	MPSLD		Loading mps (HWW7 or overlay)
	FMP		Microprogram loaded flag
	FHMP		Hardwired microprogram flag
	SPX	00,01	ARU Scratchpad ext. bits
	AT	00,01	ARU Arithmetic type.
	DS		ARU Double/Single length shifting.
	JF		ARU Jump Flag.
	JFA		ARU Jump Flag A
	SA		ARU Address SPAD from AN.
	RE		ARU Register Extension
	LF		ARU Link register from microprogram bits.
	SPOS		ARU Sign Positive (Dec. arithmetic).
	CY		ARU mill carry flag.
	PM		Program Mask (PSR)
	P+C	00,01	ARU Multiplier.
	CS		ARU Carry Save.

Row 8 (14R)	WA	00-31	AGU WA register.
	EMFV		Emulation Floating point overflow
	V		Common overflow
	CC	00,01	Common CC
	RAZ	00,01	Buffer ACC size
	ROZ	00,01	Buffer Operand size
	ARUTWIST		ARU TWIST Stat.
	RAF	00-06	ARU Function Register.
	FBOOTS		Hardwired Bootstrap.
	LOAD DEC	00-03	Direction bits.
	GMPS AD DEC	00-02	AGU Microprogram Address selection.
	MPS DATA	00-13	AGU MPS Data Buffer (see Row 9).
Row 9 (15R)	WB	00-31	AGU WB register.
	AV		ARU Overflow
	CC	00,01	ARU CC
	NEW AZ	00,01	ARU New Instruction ACC size.
	OLD AZ	00,01	ARU Previous Instruction ACC size.
	MPS DATA	14-44	AGU MPS Data Buffer.
Row 10 (16R)	SB	00-31	AGU SPAD output highway.
	SB	P0-P3	AGU SPAD output highway parity
	MPS CURR ADD.	00-11,P	AGU Microprogram Current Add.
	MPS ACC ADD.	00-11,P	AGU Microprogram Access Add.
	NULL		Null Beat (AGU)
	FADD		Forced Address (AGU).
	FWD		
	STOLK3		AGU Lockout.
	LKS1		AGU Lockout.
	LKS2		AGU Lockout.
	ADD LKS		"
	RUN LKS		"
	STL1		"
	STL2		"
Row 11 (17R)	K	00-31	AGU K highway.
	DT	00,01	Descriptor Type.
	DZ	00-02	Descriptor Size.
	A		A bit.
	USC		Unscaled.
	BCI		Bound Check Inhibit.
	FRAM	00-06	Function RAM Addressing.

	KRAM	00-06	K Field RAM Addressing.
	IRAM	00-06	Descriptor RAM Addressing.
	vi Access	00-02	Volatile Index Address Selection.
	VI ADD	00-07	Volatile Index Addressing.
Row 12 (18R)	L	00-31	$\overline{\text{AGU L}}$ highway.
	FSP 2 & 3		AGU SPAD Flags.
	SPAD ADD	00-03	" " Addressing
	OTB		Valid Stats. (Microprogram Address valid for replaced jumps if required).
	GOB		
	DTB		
	DZB		
	INTB		
	RLOTB		
	REALER		
	ARUSTP		
	AMP AD DEC	00-02	ARU Microprogram Address selection.
	REPLMT		
	FPNXT		Next ARU func. is floating point.
	RFB		AGU/ARU Interlocks.
	RBB		" "
	AAR		" "
	OPINT		Operand in Internal Format.
	ACINT		ACC in Internal Format.
	AOK		
	BUF 2F		Association Address
	SSNEQ		Stack Segment Number Equivalence
	ISL		Instruction Slave — Slave hit
	SSL		Stack slave — Slave hit
	IB		Slave last hit
	GBM		Slave last hit
	GBL		Slave last hit
	RBM		Slave last hit
	RBL		Slave last hit
	LKS 1		ARU Lockout.
	LKS 2		"
	PLKS		Pipe Locks

Row 13 (19R)	Q	00-31	AGU Q highway.
	FSP0 & 1		AGU SPAD Flags
	MPS	00-35	ARU Microprogram word.
Row 14 (20R)	GBM	00-31, 0P-3P	AGU GB Most.
	MPS CURR ADD	00-11, P	ARU Microprogram current address.
	MPS ACC. ADD	00-11, P	ARU Microprogram Access address.
	WFL		ARU Wait for Literal.
	FADD		ARU Forced Address.
	VIADD	00-06	ARU Volatile Index Address.
Row 15 (21R)	GBL	32-63	AGU GB Least.
	GBL	04-07	AGU GB Least Parity
	TA	04-29, P	Store Address, (Real Address).
	BYTE FUNC	00-07, P	
Row 16 (22R)	PORT 0 SEINT		Direct wired interface interrupts.
	PORT 0 EXINT		
	PORT 0 OPINT		
	PORT 1 SEINT		
	PORT 1 EXINT		
	PORT 1 OPINT		
	PORT 2 SEINT		
	PORT 2 EXINT		
	PORT 2 OPINT		
	PORT 3 SEINT		
	PORT 3 EXINT		
	PORT 3 OPINT		
	MVSI		Masked Virtual Store Interrupt.
	MPE		Masked Program Error.
	MSCI		Masked System Call Interrupt.
	MOUT		Masked Out Interrupt.
	MXC		Masked Extracode.
	RGN	24-31	AGU $\overline{GN}$
	RGNZR		AGU GN bits 8-23 = zero.

Row 16
Cont.

ACCESS E		Store Access Execute.
ACCESS W		Store Access Write.
ACCESS R		Store Access Read.
APF	03-11	Access Protection Field bits.
ACR	00-03	Access Control Register.
PERF		Permission Fail.
MEQ		Multiequivalence.
TAC		ATU Accept (Hit).
UMS		Update Miss (Use bits).
MS		Miss.
MISS		
PAGEI		Paged segment address.
VAM		Virtual Address Mode.
SIP		Search In Progress (TS).
LOAD VIR		Load Virtual Address.
LOAD PAP		Load Page and Permission bits.
LOAD RRE		Load Real Even address.
LOAD REO		Load Real Odd address.
WD M, L		
CPR	P0-P2	ATU CPR Pointer.

Row 17 (23R)	SSE	Interrupt Register
	GPE	
	VSI	
	EP	
	OUT	
	XC	
	SE	
	SGSE	
	RTC	
	XACT	
	HRI	
	APE	
	IT	
	IC	

Row 17 Cont.	FKI	Function K and Indirect RAMS	Parity Fail Stats.
	ASE	ARU System Error	
	IB	Instruction Buffer	
	RC	ARU control	
	GC	AGU control	
	GK	K highway	
	GL	L highway	
	GQ	Q highway	
	GCY	Carries	
	GMISC	AGU Misc.	
	SSD	Stack Slave Data	
	SSA	Stack Slave Address	
	ISD	Instruction Slave Data .	
	ISA	Instruction Slave Address	
	SMAC		
	SDIE	Software DIE	
	DIE	Hardware DIE	
	TRANS		
	CHECK		
	MODE		
	PERMIT		
	BUSY	Current stats. of ATU	
	RIP		
	REQ		
	APHIP	ARU Photograph in Progress	
	CASS	Cassette is Busy	
	FEM	Emulation mode flag.	
	EM 0-3	Emulation mode.	
	H BUSY	Hash Busy	
	STREQ	Store Request	Requests from input device
	MPREQ	Microprogram request	to main and Microprogram store.
	OFFLINE		
	PERI	Perifail	Diagnostic Unit
	STORE	Store Fail	Input Device
	UNSERVED		Fails
	CNT	Count Fail	
	MPSINH	MPS Inhibit Fai.	
	RAM Add. X0-3	ATU RAM Address.	
	Y0-3		
	Y01,Y23	ACR use bit checks RAM address since only one ACR use bit is held for each Virtual Address Pair (even and odd).	

Row 18 (24R)	WD	00-63, P0-P7	Write Buffer store.
Row 19 (25R)	ARU COPY BUFFER	00 - 11	
	AGU COPY BUFFER	00 - 11	
	1900 EM LINK	00 - 11	1900 Emulation Link (AGU)
	AGU SR	00 - 11	AGU SUBROUTINE
	AGU LR	00 - 11	AGU Link
	INHAM	Inhibit Hamming Interrupt	CW STATS
	INSTO	Inhibit Main Store	
	IRTY	Inhibit Retry	
	ISRS	Inhibit Successful Retry Reporting	
	ISTSL	Inhibit Stack Slave	
	IINSL	Inhibit Instruction Slave	
	ICPRS	Inhibit Current page/segment Registers	
	IPHOT	Inhibit Photo	

External Monitor Strip

OPTINT	0,1	Peripheral Interrupt
IDLE		
OPERAND	14-31	
HMP		Hard Microprogram
GMPADD	8-11	AGU Microprogram Address
SEINT	0,1	System Error Interrupt
SMACFL		SMAC Fail

HANDKEYS

The handkeys are arranged in three rows A, B and C and are depicted on OD61 of document 65/94562.

Row A Handkeys 1 - 32 are used for setting up Image Store data.

Handkeys 33 - 36 vary the OCP Timing Margins as follows:

a) Key 33 AGU FAST down - All AGU timing speeded up by 5%
b) Key 34 AGU SLOW down - All AGU timing slowed down by 20-25%
c) Key 35 ARU FAST down - All ARU timing speeded up by 5%
d) Key 36 ARU SLOW down - All ARU timing slowed down by 20-25%

Note: The results of setting AGU FAST and AGU SLOW or ARU FAST and ARU SLOW is indeterminate.

e) All four switches in centre position - timing at nominal speed.
f) Key 33 up - Individual AGU timing pulses as determined by a decode of the remaining 3 switches speeded up by a constant 5 n Sec (see table 1).

Switches			AGU Timing Pulse
KEY 34	KEY 35	KEY 36	Speeded up by 5n Sec.
Centre	Centre	Centre	T08TM
Centre	Centre	TDEC2	T14TM
Centre	TDEC1	Centre	T17TM
Centre	TDEC1	TDEC2	T19TM
TDEC0	Centre	Centre	T12DF
TDEC0	Centre	TDEC2	T12TM
TDEC0	TDEC1	Centre	T17GMIL
TDEC0	TDEC1	TDEC2	Conditional Jump

Table 1. AGU timing Pulse Margin Speed Up

g) Key 33 centre - Individual ARU timing pulses as determined by a decode of the remaining 3 switches speeded up by a constant 5n Sec (see table 2).

Switches			ARU Timing Pulse
KEY 34	KEY 35	KEY 36	Speeded up by 5n Sec.
Centre	Centre	Centre	All AGU and ARU Timing Nominal
Centre	Centre	TDEC3	T11DF
Centre	TDEC1	Centre	T10TM
Centre	TDEC1	TDEC3	T08RTIM
TDEC0	Centre	Centre	T12TIM
TDEC0	Centre	TDEC3	T12RTIM
TDEC0	TDEC1	Centre	T17RTIM
TDEC0	TDEC1	TDEC3	T17MILL

Table 2. ARU Timing Pulse Margin Speed Up

Row B This row of keys enables the OCP to stop on a specified address, stopping on either microprogram equivalence (handkeys 1 - 12) or, on PC and ZA equivalences (keys 1 - 31). The specific equivalence on which the OCP stops is determined by the four keys situated at the extreme right-hand end of this row (keys 33 - 36).

MISC STOP, Key 32 down, stops the OCP when the AGU Miscellaneous Function 'STOP ON MISC' is set.

Stop on Microprogram loaded/PC; Key 33 enables the OCP to be stopped when the microprogram has completed loading by detecting #F (Stop character) in the direction bits. The other position of the key "Stop on PC equivalence" stops the OCP immediately equivalence is detected between the bits set-up on the handkeys and PC providing that "Stop on AGU/ARU Microprogram address" is not set. The OCP will resume running when the key is returned to the centre off position.

Stop on - ARU/AGU microprogram address; Key 34 enables the OCP to be stopped when bits 00-11 of the ARU/AGU microprogram address are equal to the bits set up on the keys. The OCP will resume running when the handkey is returned to its centre-off position.

When both the "Stop on PC" Keys 13-31 and "Stop on AGU microprogram address" 1-12 are set, then the OCP will only stop when equivalence is detected between these conditions and that set up on the keys.

ZA Read/ZA All and ZA Write/ZA Execute; Keys 35 and 36 enable the OCP to be stopped when ZA (which normally contains the virtual address) is equal to the bits set on the keys. The OCP will resume running when the appropriate key is returned to its centre-off position.

Keys 1 - 12 can also be used to set up the Port, Trunk and Stream when doing a Bootstrap or dump (Row C handkey 34).

FEM, Key 13 down, stops on selected address (Keys 1 - 12) when in emulation mode and stops on selected address in normal mode when key in neutral position.

A further facility exists on this row in that the group of keys at the left-hand end can be set to force either the ARU K (AK 00-02) L (AL 00-02) and KX (AKX 00-02) highways and the ARU scratchpad (ASP 00-03) and AC→AK, or alternatively the AGU Scratchpad Flags (0-3) and AGU Scratchpad, and J Highway. The condition to be displayed is dependant upon the setting of the Display ARU/ Display AGU handkey (key 31 Row C).

Row C

KEYS

1	– ENG	Enables Engineers panel and disables OPER
2	FORCE IT INHIBIT IT	Force Interval Timer interrupt Inhibits interrupts from the Interval Timer and RTC
3	RAM ACR0	Force Real Address Mode Force ACR0
4	STOP ON SMAC FL IGNORE SMAC FL	Allows OCP to stop on unrecovered SMAC Fails Allows OCP to ignore unrecovered SMAC Fails
5	STOP ON SE FL IGNORE SE FL	Stops OCP on System Error Fail Allows OCP to ignore System Error Fail
6	INHIBIT CPR EX INHIBIT CPR ALL	Prevents the CPR's being used during execute accesses Prevents the CPR's being used during all store accesses
7	– INHIBIT PORT ACT	Prevents the OCP from taking any action as a result of receiving an ACTIVATE
8	– INHIBIT PORT INT	Prevents the OCP from raising an interrupt as a result of receiving a port interrupt.
9	– STOP ON SACTOUT	Causes OCP to stop on SAC Time out
10	– INHIBIT IC	Inhibits the instruction counter interrupts
11	STOP ON TIMEOUT IGNORE TIME OUT	Causes OCP to stop on any time out Allows OCP to ignore any time out

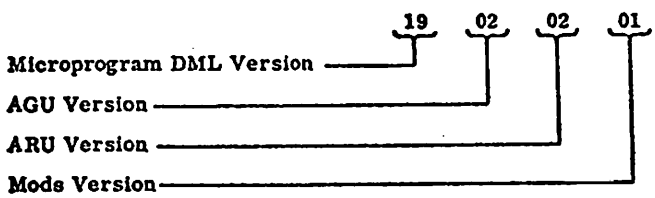
KEYS

12	RESET FAILS INHIBIT PHOTO	Resets any outstanding fail Allows the system Error Interrupt routine to omit the Photo of the OCP hardware
13	— INHIBIT INSTSL	Inhibits the Instruction slave
14	RESET LOCKOUTS INHIBIT INTLKS	Reset any Lock outs (or any timing interlocks) Allows AGU and ARU to run irrespective of any interlocks that may be set.
15	— INHIBIT STK SL	Inhibits the Stack Slave causing all read accesses to come from main store.
16	— INHIBIT HAM INT	Inhibits any Hamming Interrupt
17	INHIBIT SRR INHIBIT RETRY	Inhibits successful Retry reporting Allows the system Error Interrupt to by pass the hardware retry.
18	— ENABLE SMAC FRZ	This key allows the OCP general reset (FREEZE) to be passed via a Port to the SMAC.
19	DUMP —	Results in a PAW Function of Dump being sent to the Controller selected on the Keys of Row B when the RUN Key (35 Row C) is set OCP then stops.
20	— STOP ALL	Allows Stop on nulls (AGU and ARU)
22	STOP AGU AGU LOOP	Stop AGU Clocks. Inhibits the strobing of the AGU microprogram data buffers, thus enabling a specific beat to be repeated indefinitely.
23	STOP ARU ARU LOOP	Stop ARU clocks. Inhibits the strobing of the ARU microprogram data buffers thus enabling a specific beat to be repeated indefinitely.

25	— EKS	This key is the M.S.B of the Engineers Facility Field and also the drop through Idle
26-29	EF00 01 02 03	These keys have two functions:- (X) They are looked at, at Microprogram load time (IPL), and if the decode is #5, the VAR Register is loaded from the Image Store Keys Row A. (Y) These four Keys and EKS (Key 25) provide a means of forcing several functions manually provided the Engineers facility (Key 32 Row C) is operated. The OCP should be at Real OTB. Key 35 Row C should be in OI position. The Engineers facility is performed by setting the decode, then pressing and releasing the Engineers Facility Key (Key 32 Row C), followed by the operation of the GO Key (Key 36 Row C). The facilities provided are as follows:-

Engineers Facilities.

0		No Action
1	PC JUMP	Jump to Address on Image Store data keys Row A as per address mode, Virtual or Real.
2	MPVERS	Microprogram Version displays on the AGU Register WB display on Row 9. The decode is Hexadecimal. For example:



3-7		No Action
8	READ	Read from virtual address in Store. The address is set on Image Store Keys Row A. The information read is displayed in Registers GBM and GBL Rows 14 and 15.

9	READ +	Read from virtual address is store. The address is set on Image Store Keys Row A. The information read is displayed in Registers GBM and GBL Rows 14 and 15. EKS key being pressed and released increments the virtual address by 2 words and the new information is displayed in GBM and GBL Registers. The microprogram can be returned to real OTB by returning EF 00-03 keys to neutral and pressing and releasing EKS Key.
A	Read R	As 8 (READ) but the Real Address Mode Key (Key 3 up Row C) operated.
B	Read R +	As 9 (READ +) but the Real Address Mode Key (Key 3 up Row C) operated.
C	WRITE	Write to the virtual address set on the Image Store Keys Row A upon the operation of the GO Key (Key 36 Row C). The machine will now wait for data to be set on the Image Store Keys. When EKS Key is operated this data is written into the virtual address in store
D	WRITE +	Write to the virtual address set on the Image Store Keys Row A upon the operation of the GO Key (Key 36 Row C). The machine will now wait for data to be set on the Image Store Keys. When EKS key is operated this data is written into the virtual address in store. Further press and releases of the EKS key increment the address by 2 words and write the data on Image Store Keys. The microprogram can be returned to real OTB by returning EF00-03 keys to neutral and pressing and releasing the EKS key.
E	WRITE R	As C but Real Address Mode key operated (Key 3 up Row C).
F	WRITE R+	As D but Real Address Mode key operated. (Key 3 up Row C).
10	MOVEOVER	Move overlays from existing to new area of store set on Image Store keys (Row A).
11	FOTO	Force Photo, done automatically by this key.
12	READ INST SLAVE	Read the line of the Instruction Slave defined on Image Store Keys, and appears on monitor lights GBM and GBL Rows 14 and 15.
13	READ STACK SLAVE	Read the line of the Stack Slave defined on Image Store Keys, and appears on monitor lights GBM and GBL. Rows 14 and 15.
14,15		No Action.

16 READ AND WRITE SAC AND SMAC I.S.

To read set the Engineers Facility keys, set the image store address as defined below *, and perform the functions described in paragraph (Y), preceding the Engineers Facilities. The information in GBM is the Image Store address which has been set up and in GBL is the information Read.

To Write set up Image Store Keys Row A, perform the Engineers Facility operation described in paragraph (Y) but after the GO key has been pressed the OCP will wait for data which is to be set up on Image Store Keys. EKS key is pressed and released this causes the Image Store write action to be completed.

* Image Store Keys Row A.

Bit 0 :- 0 Read, 1 Write

4,5:- Both down :- SMAC; 5 only :- SAC; No keys operated:- SAC Trunk.

SMAC
- Bits 8-15 SMAC number
- Bits 16-31 SMAC Image Store Address (see N.R.S.D 4,2,3 G)

SAC
- Bits 8-11 Port number of SAC
- Bits 16-31 The Image Store Address

17 No Action

18 WRITE SPADS

On Image Store keys 24-27 put the S.P. Flags, and on keys 28-31 put the S.P. line number. The Image Store Engineers Facility action described in paragraph (Y) is performed. The data to be written to the Scratch Pad is set on the Image Store Keys. EKS key is then pressed and released.

19 UPDATE SP

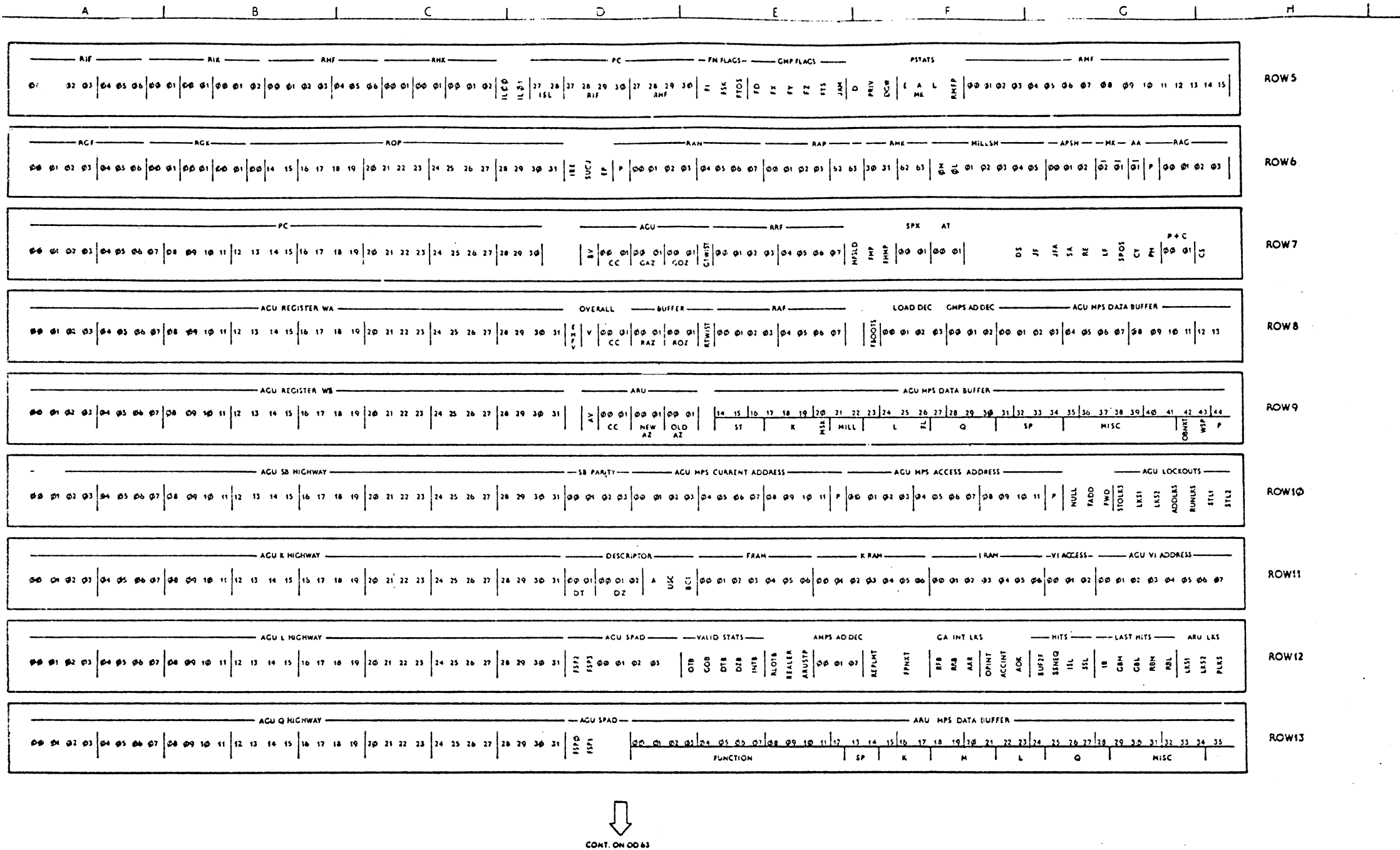
This updates the visible Registers to the current machine state automatically

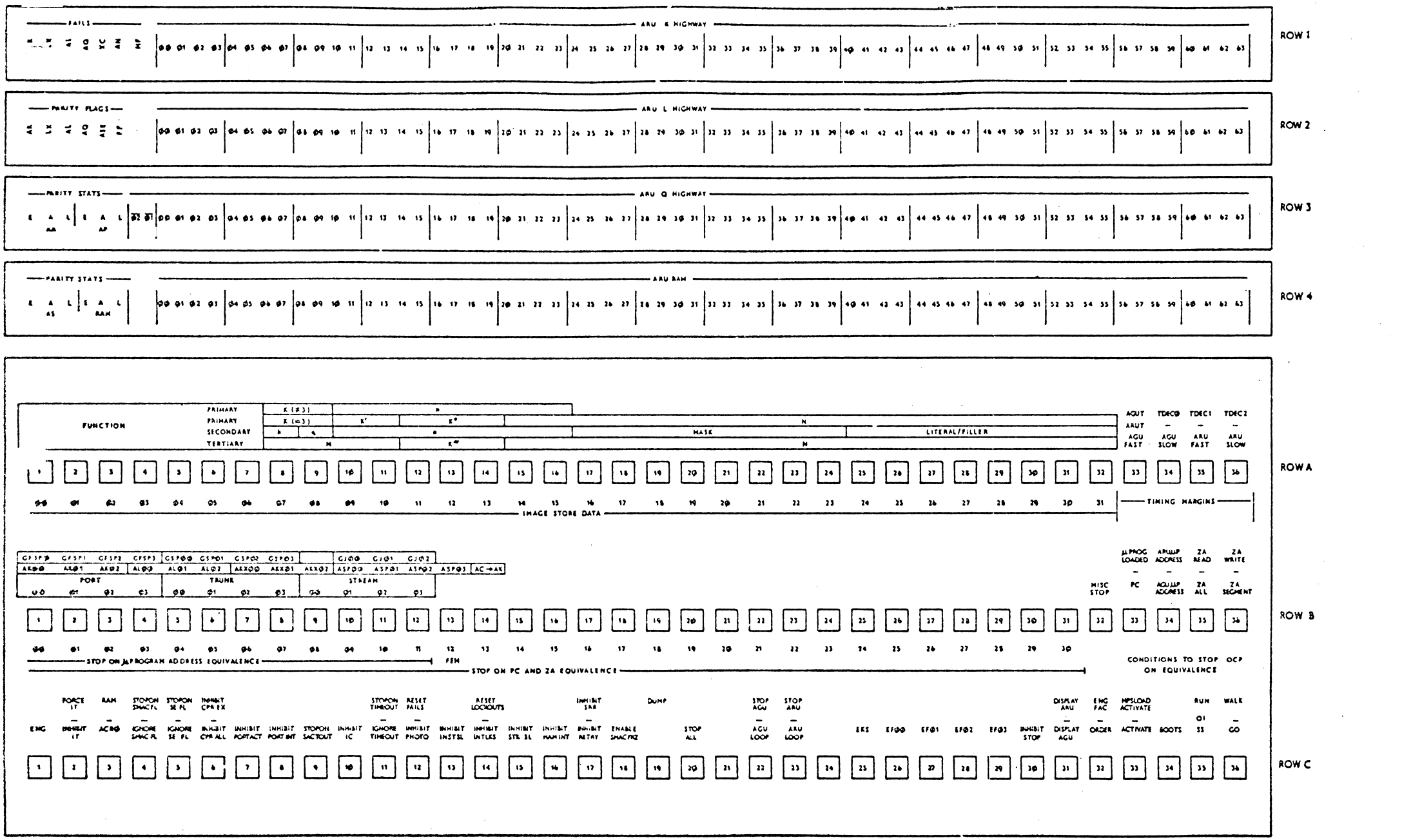
e.g. ACS, CC, OV in PSR

SP SA (IT Copy)
SP SW (A0 Copy)
SP SX (A1 Copy)
SP SY (A2 Copy)
SP SZ (A3 Copy)
SP PC
SP SD (IC Copy)

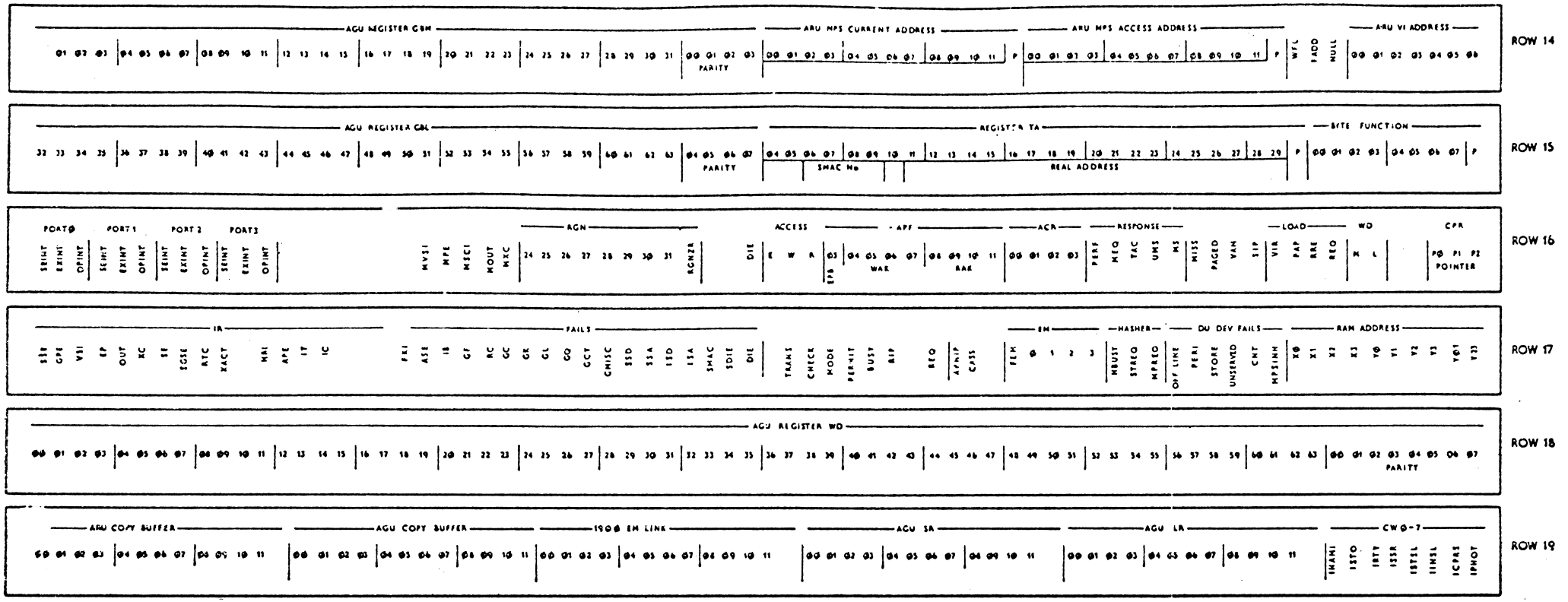
30	INHIBIT STOP	Used in conjunction with stop keys to provide Engineers Scope trigger.
31	DISPLAY ARU DISPLAY AGU	This key causes the Register(s) selected by the keys on row B to be placed on the highways which in turn are displayed on monitor lamps.
32	ENG FAC ORDER	Enables the Five Keys 25-29. The ORDER position allows the primitive interface order set up on ROW A to be obeyed. If only one order is required the RUN key (35 Row C) is placed in the appropriate position and the GO Key is pressed once.
33	MPSLOAD ACTIVATE	When operating the MICROPROGRAM LOAD switch it is assumed that the microprogram is in the main store starting at #100 BYTES, the RUN switch (Key 35) should also be set. The microprogram is then loaded and entered and if it is a normal Microprogram it carries out a register load from #80 BYTES etc.
33	ACTIVATE	The ACT position of this switch causes an entry to the microprogram such that if a normal microprogram is in, a register load from #80 BYTES etc. is carried out when RUN is set.
34	BOOTS	Operation of this key results in a PAW function of IPL being transmitted to the controller selected by the Keys of Row B. On receiving an interrupt from the controller the OCP loads its microprogram etc.
35	RUN	The RUN position allows the clock to run until it is stopped by a stop condition or RUN is switched off. The conditions for stopping are various and are as follows. 1. The stop conditions described under ROW B 2. System error with stop on System Error or system Error mask set. 3. Inhibit time out and the OCP is waiting for something. 4. AGU and ARU only with the interlock functioning.
35	OI	One instruction allows a single instruction for each operation of WALK/GO key.
35	SS	Single shot allows a single microprogram instruction for each operation of WALK/GO key.

36	WALK	A 16 μ sec clock used in conjunction with OI and SS.
	GO	A Single Shot used in conjunction with OI and SS.


A
B
C
D
E
F
G
H
ROW5
RIF
RIK
RHF
RHK
PC
FN FLAGS
GMP FLAGS
PSTATS
AMF
ROW6
RGF
RGK
ROP
RAN
RAP
AMK
MILLSH
APSH
MK
AA
RAG
ROW7
PC
AGU
RRF
SPX
AT
P+C
ROW8
AGU REGISTER WA
OVERALL
BUFFER
RAF
LOAD DEC
GMPS ADDEC
AGU MPS DATA BUFFER
ROW9
AGU REGISTER WB
ARU
AGU MPS DATA BUFFER
ST
R
MSK
MILL
L
FL
Q
SP
MISC
OBNXT
WSP
P
ROW10
AGU SB HIGHWAY
SB PARITY
AGU MPS CURRENT ADDRESS
AGU MPS ACCESS ADDRESS
AGU LOCKOUTS
NULL
FADD
FWD
STOLKS
LKS1
LKS2
ADDLKS
RUNLKS
STL1
STL2
ROW11
AGU K HIGHWAY
DESCRIPTOR
FRAM
K RAM
I RAM
VI ACCESS
AGU VI ADDRESS
ROW12
AGU L HIGHWAY
AGU SPAD
VALID STATS
AMPS ADDEC
GA INT LKS
HITS
LAST HITS
ARU LKS
ROW13
AGU Q HIGHWAY
AGU SPAD
ARU MPS DATA BUFFER
FUNCTION
SP
K
M
L
Q
MISC
CONT. ON 00 63



NOTE:
FOR CONNECTIONS BETWEEN M
AND BETWEEN MONITOR DIS
FOR SIGNALS FROM WANDERI


A
B
C
D
E
F
G
H
ROW 14
AGU REGISTER GBM
ARU MPS CURRENT ADDRESS
ARU MPS ACCESS ADDRESS
ARU VI ADDRESS
PARITY
P
WFL
FADD
NULL
ROW 15
AGU REGISTER GBL
REGISTER TA
BYTE FUNCTION
PARITY
SMAC No
REAL ADDRESS
ROW 16
PORT0
PORT1
PORT2
PORT3
SEINT
EXINT
OPINT
AGN
ACCESS
APF
ACR
RESPONSE
LOAD
WD
CPR
POINTER
ROW 17
IR
FAILS
EM
HASHER
DU DEV FAILS
RAM ADDRESS
ROW 18
AGU REGISTER WD
PARITY
ROW 19
ARU COPY BUFFER
AGU COPY BUFFER
1900 EM LINK
AGU SA
AGU LR
CW0-7
OPINT
IDLE
OPERAND
CMPADD
SEINT
SMAC #1
EXTERNAL MONITOR STRIP

EMAS 2900 HARDWARE NOTE

No: 3
Date: 13/12/79

How to Force a Program Error Interrupt from the Handkeys

Before a dump can be usefully taken the machine must be at IDLE "DEAD". This state is reached after most hardware and software errors. However, if the machine is not at IDLE "DEAD" an error should be forced, as follows:

For the 2960 (SM11, using TLOE/8):

On the ECP, type:

```
DW 9FFC
WMA 0 E
GO
```

For the 2970:

1. Off "RUN"
2. "ENG" down
3. Handkeys (top row) to ZERO
4. One tick on "GO" (usually, but more ticks may be necessary) until the RLOTB light comes on
5. "ORDER" down
6. Press "GO" until no lights on in RGF (2nd row of lights from top)
7. "ORDER" central
8. "RUN" - machine goes to IDLE "DEAD"

For the 2980:

1. Set switches as follows:

SMGO	UP	(Row 1 Key 1)
S.INST.MODE followed by S.SHOT MODE	DOWN/UP	(Row 6 Key 2)
I1 STOP	DOWN	(Row 3 Key 7)
STOP ON FAIL	UP	(Row 5 Key 4)
INH.ORD.STOP	DOWN	(Row 5 Key 9)

   These are the only switches that should be set, apart from the deck TRUNK/STREAM switches. Unset any others.

2. Turn to Frame 01 (Critic and Modifier Dataflow) on monitor display.
3. Set Serial Monitoring address keys to Frame 1, Line 3.
4. Set bit 17 on DATA-KOD keys.

5. Press SET REG (Row 1, Key 4 - UP). Check that lamp FSEI on Line 3 (bit 17) comes on.

6. Turn to Frame 10 (Modification and B Arithmetic Stage Microprogram) on monitor display.

7. Set RUN (Row 6, Key 2 - CENTRAL).

8. Press GO (Row 6, Key 1 - DOWN). Check that machine stops with I1 (Line 7, bit 4) lamp lit.

9. Turn to Frame 21 (SAC trunk links E, F, G, H) on monitor display.

10. Rest I1 STOP (Row 3, Key 7 - CENTRAL).

11. Press GO (Row 6, Key 1 - DOWN) - machine goes to IDLE "DEAD".

R.D. Eager
J.F. Livingstone
P.D. Stephens
J.K. Yarwood

EMAS 2900 HARDWARE NOTE

No: 4
Date: 19/12/77

Hardware Testing

A process, ENGINR, exists to be used for running hardware tests. Currently two tests exist:

a) A test of the VMY instruction accessing the B register and data which goes across a page boundary. This used to give an erroneous bound check on the 2970 when a page fault occurred during its execution; it has now been corrected. The test is preserved for use on other 2900 machines. To run it, type:

```
COMMAND: RUN VMYBY

DO YOU WANT SECOND PAGE IN CORE?
Y/N: N or Y

VMY B WORKED OK.
```

Note that the program should work whether or not the second page is in core. If the fault exists the program will work when the reply is 'Y', but will fail with a band check if the reply is 'N'.

b) RAND READ

This is a program based on RAND READ on System 4 EMAS. It can be used to test up to 4 disk drives. The disks are referred to by their FSYS numbers - e.g. PETE01 is disk 1, EMAS10 is disk 10.

The program is run thus:

```
COMMAND· RANDREAD

NO OF DISKS:          reply 1-4

FSYS NOS. OF DISKS:   reply with FSYS numbers

Q SIZE PER DISK:      reply 1-16, specifying number of transfers to
                      be PONned to each disk at once

READS/DISK:           reply with number of READs to be done
```

When the specified number of reads have been completed, the number of faults, cumulative since the start of the command, are reported and the user is then invited to continue. The reply should be Y to continue or N to stop the tests. If the user replies with Y, the READS/DISK: prompt is given again; the other parameters are held at their previous values.

Roderick McLeod

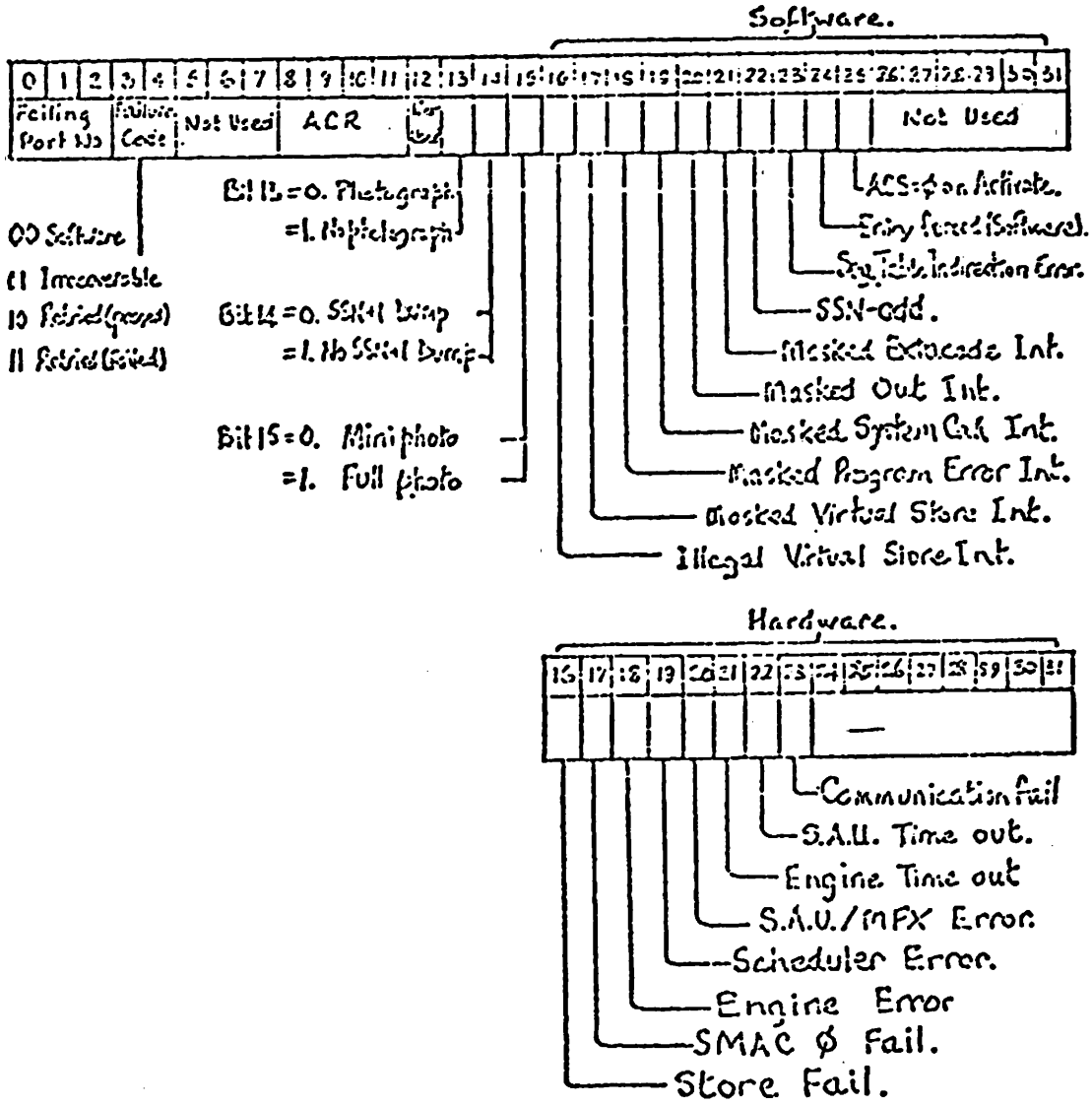
System Error Interrupt Parameters for 2960, 2970, 2980

This note is taken from a badly-Xeroxed copy of ICL document SYSB-22-0233.

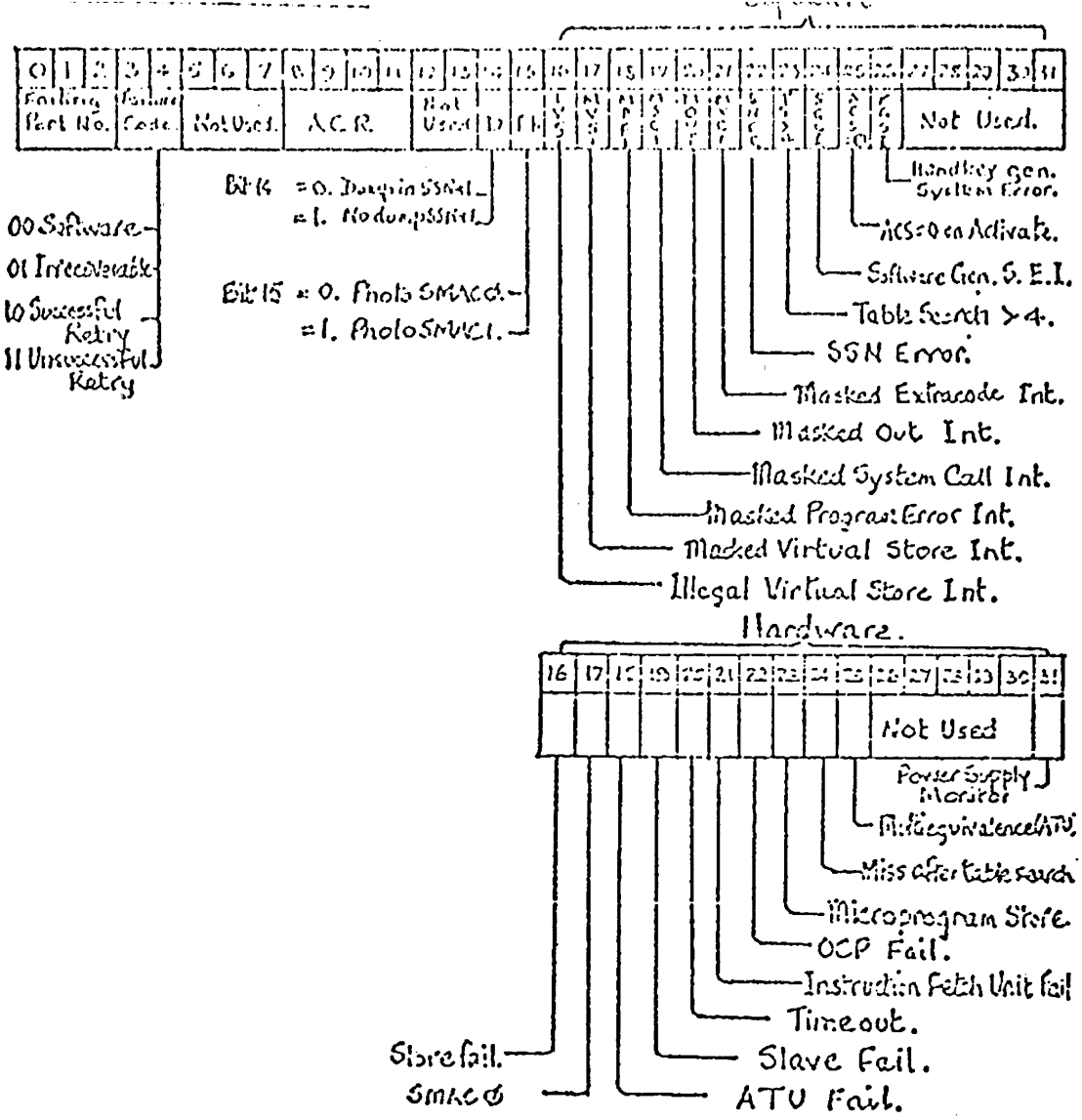
The System Error Interrupt Stack

The system error is a stack switching interrupt and the code of SEI Analyser is entered with its LNB at the stack base. Word 0 contains the stack segment number (in the current implementation this is public segment 8198). Words 1 and 2 are zero and words 3 and 4 point to the Procedure Linkage Table (PLT) of the compilation module containing SEI Analyser. Word 5 contains the SEI parameter as stacked by the hardware interrupt routine and word 6 is the segment number of the interrupted stack.

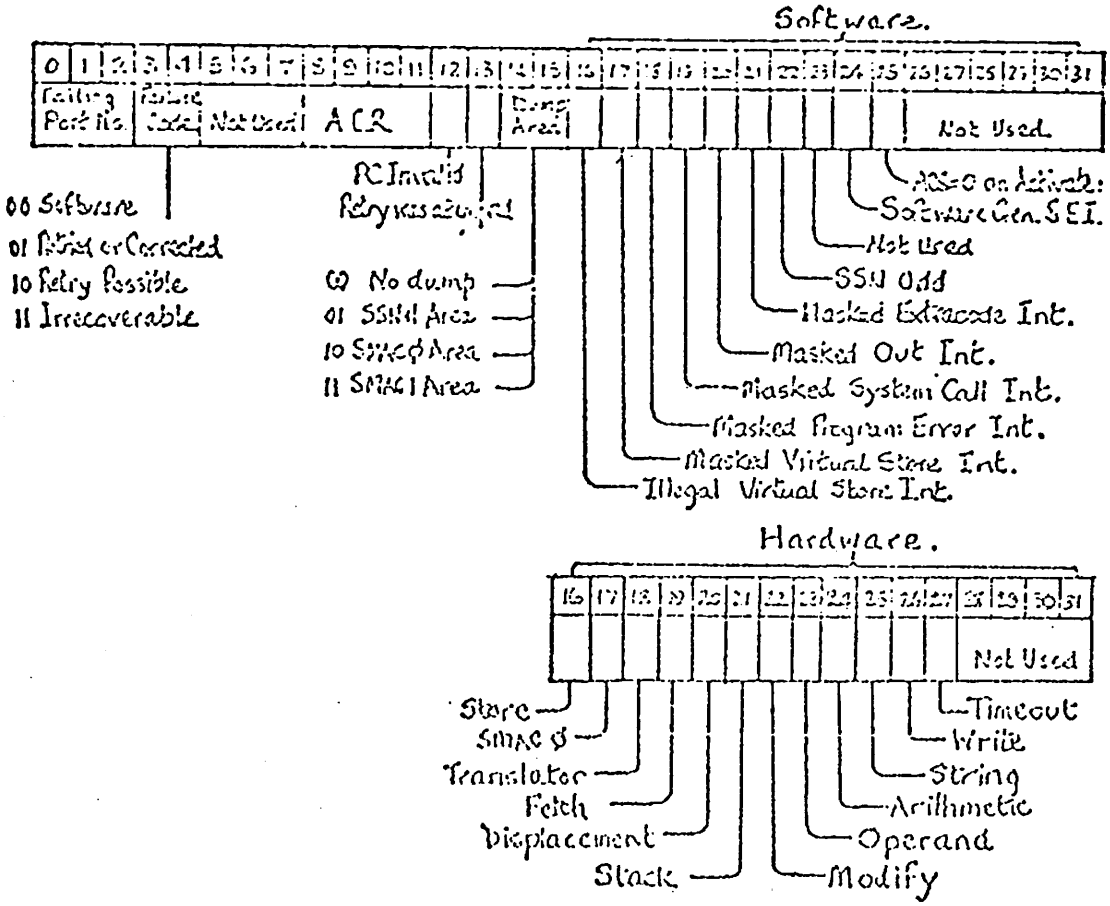
SEI Parameter for 2960



The parameter for interrupts other than on the current OCP port will look like an empty software failure parameter (i.e. bits 16-31 not used).



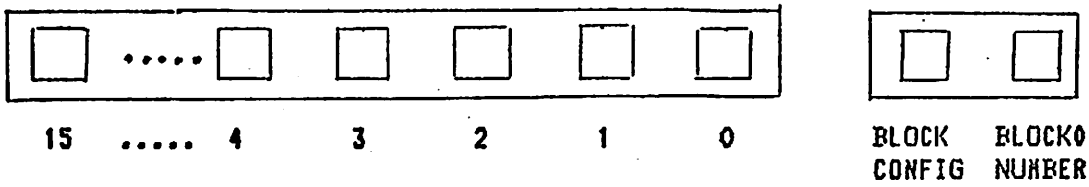
SEI Parameter for 2980



No: 6
Date: 11/7/78

2970: How to Reconfigure the Store on a SMAC

Use the bottom row of (mostly) blue keys in the store cabinet:



The BLOCK0 NUMBER key is grey, all other keys on this row are blue. Each 128 Kb block required to be on-line should have its corresponding key (0-15) pressed down. Effect the reconfiguration by pressing (and releasing) the adjacent BLOCK CONFIG key. The BLOCK0 NUMBER refers to the lowest numbered on-line block (generally real block 0). If the reconfiguration changes the lowest numbered block then the new BLOCK0 number should be set on the four grey keys on the row above the block configuration row and the BLOCK0 NUMBER key pressed and released. The fifth row of lights on the Store cabinet displays the current block configuration and BLOCK0 number.

N.B. The Store need not be contiguous except that the EMAS Supervisor loader requires blocks 0 and 1 of SMAC 0 to be configured on-line.

John Maddock

No: 7
Date: 9/10/78

2950: Notes on Transfer Control Blocks (TCBs) for People Who Are Used to the GPC

This Note is intended as a commentary on pages 30-40 of the ICL Product Specification document PSD 2.5.3, an extract of which is available on request. The diagram is taken from the document.

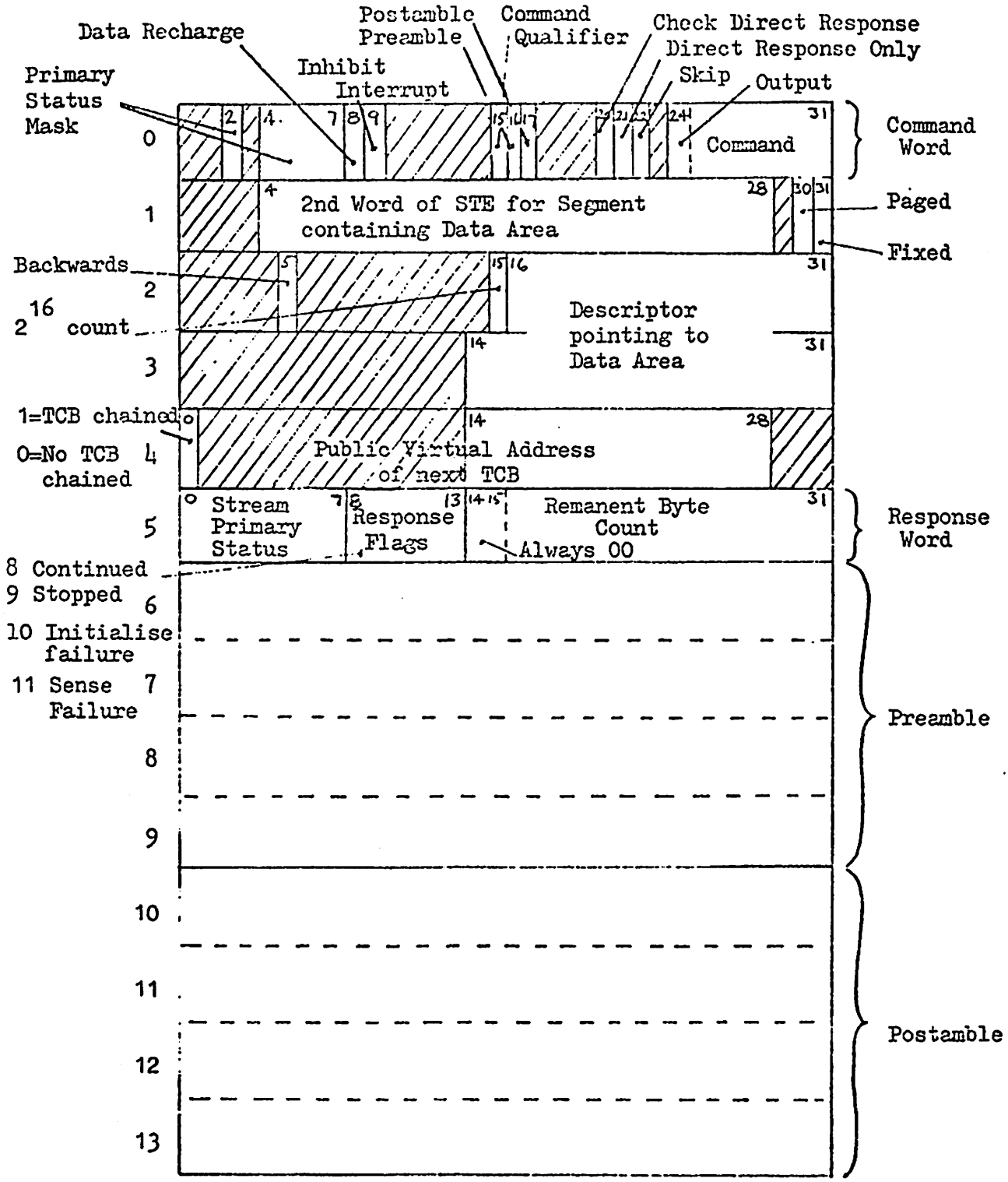
TCB Word 0

bits 0,1	not used
bit 2	if set, suppresses termination on "attention"
bit 3	not used
bits 4-7	suppress long block, short block, condition X, condition Y ≡ bits 8 to 11 of logic block entry
bit 8	data recharge from next TCB: equivalent to bit 4 of LBE
bit 9	inhibit interrupt: converse of bit 3 (PCI) in LBE (could also serve for bit 2 of SAW flags in STREAM SAW in H/W comm. area)
bits 10-14	not used
bit 15	command qualifier: 0 for "device", 1 for "stream"; same as bit 15 in LBE (?)
bit 16	preamble valid: controls initialisation, like RCB word 0 bit 16
bit 17	postamble valid: controls collection of status after unsuccessful transfer
bits 18,19	not used
bits 20,21	only relevant with 1900 SI peripherals
bit 22	for read commands: don't write data to store (skip). ? Not same as LBE bit 2.
bit 23	not used
bit 24	output (this seems to be nonsense, except for stream commands)
bits 24-31	command (in actual fact bit 31 seems to signal 'output'). Whichever bit actually indicates 'output' should correspond to bit 0 of LBE

TCB Word 1

bits 0-3	not used
bits 4-28	copied from 2nd word of STE of data segment - real address of segment or page table
bit 29	not used
bit 30	paged (same as bit 1 in 1st word of STE)
bit 31	fixed - copied from 2nd word of STE; must be 1, unless you have a command to transfer no data - then it must be 0

This substitutes for the sort of information which is found in word 1 of RCB.



Notes

(i) Shaded areas are ignored by IO System but those in word 0 are reserved (for hardware use).

(ii) Word 0 must be on 2 word boundary in a Public Segment with the TCB in a contiguous area not crossing a page boundary.

The Transfer Control Block.

TCB Words 2 and 3

Data descriptor. Must be a byte or string descriptor. Only the bound and address-within-segment are significant, and only 16 bits of the bound are used - i.e., byte count in word 2 bits 16-31, and address in word 3 bits 14 to 31. A zero byte count is taken to mean 2**16. S/w should have word 2 bit 15 =1 in that case, and =0 in all others. Word 2 bit 5 must be set for "backwards" transfers (? corresponds to bit 1 of LBE).

These two words correspond to the address list entry.

TCB Word 4

Public virtual address of next TCB - only bits 0 and 14-28 are significant. Bit 0 must be 1 (public address). If it is zero (local address) the chain is terminated. Therefore this corresponds to bit 4 V bit 5 in LBE (data chain V command chain). Only address-within-segment (bits 14-28) is significant because new TCB must be double word aligned and in same segment as previous TCB.

TCB Word 5

bits 0-7	stream primary status ≡ bits 16-23 of word 0 of STREAM RESPONSE in Controller H/W Comm. Area
bits 8-13	response flags bit 8 stopped bit 9 continued bit 10 initialise failure bit 11 sense failure
bits 16-31	remanent byte count ≡ bits 14-31 of word 1 of STREAM RESPONSE

TCB Words 6-9

Preamble area

word 6	initialise data (among other things) ≡ word 6 of RCB

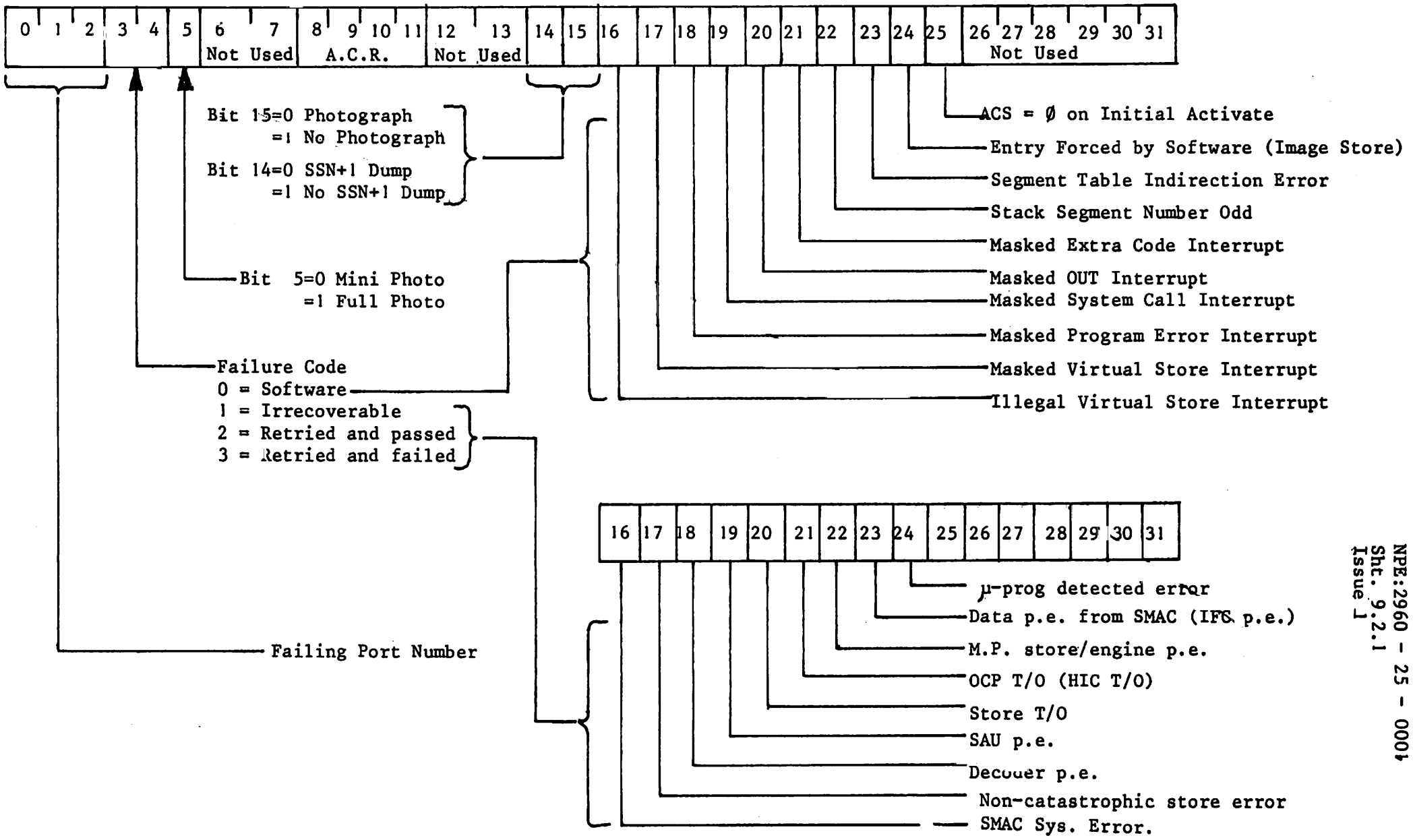
TCB Words 10-13

Postamble area. Gets sense bytes - secondary and tertiary status bytes.

J. Wexler

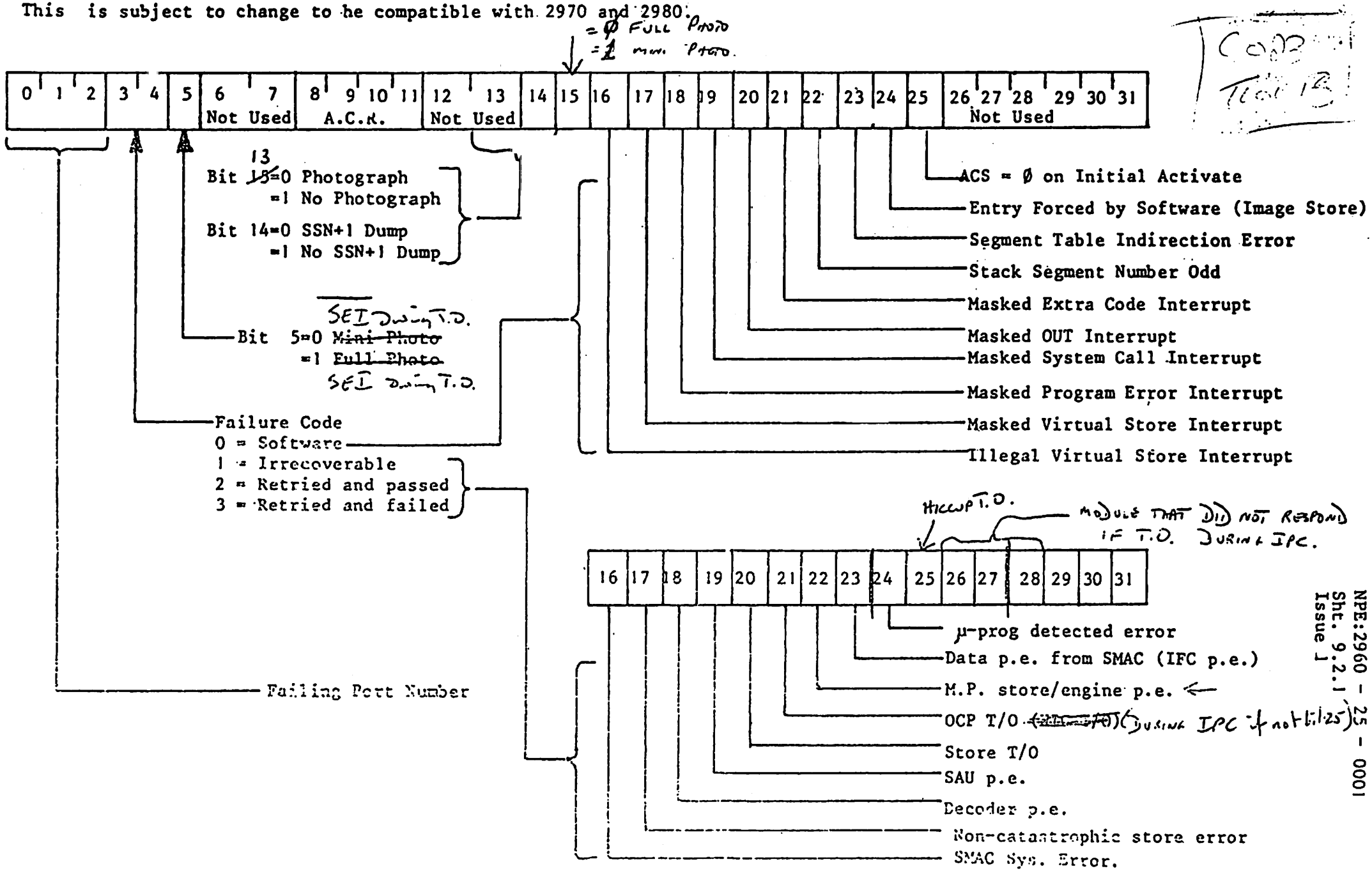
2960 5TEM ERROR INTERRUPT PARAMETER

This is subiect to change to be compatible with 2970 and 2980.



2960 SYSTEM ERROR INTERRUPT PARAMETER

This is subject to change to he compatible with 2970 and 2980.



NPE:2960 - 25 - 0001
Sht. 9.2.1
Issue 1

FIXED LOCATIONS IN WORKING STORE (N.R.)

a) Range Defined Registers Addr. by A/- or I/-

Words Ø.1	ACC Ø
2.3	ACC 1
4.5	ACC 2
6.7	ACC 3
8.9	DR Ø
10.11	DR 1
12.13	SF
14.15	B

b) Registers Addr. by C/- or C/B (For these C = # 10)

Addr. 16 (#1Ø)	Reg. SSN/LNB
17 (#11)	Prog Status Regs PSR (also STACK #1E)
18 (#12)	XNB
19 (#13)	SSR
20 (#14)	SSN
21 (#15)	LTB
22 (#16)	MBI (DETAIL SEE 3.7.3)
23 (#17)	RTCX
24 (#18)	IRS (Int Reg)(DETAIL 3.7.4)
Block 25 (#19)	PAR(Parameter)
26 (#1A)	LSTBØ
27 (#1B)	LSTB1
28 (#1C)	IM1 (Int. Mask)
29 (#1D)	IM2 (Commissioning INT. Mask)
30 (#1E)	PSTBØ
31 (#1F)	PSTB1
32 (#20)	
33 (#21)	
34 (#22)	SI PAR
35 (#23)	SIV
36 (#24)	DPC
37 (#25)	RPAR

FIXED LOCATIONS IN WORKING STORE (CONT.)

Addr.		Reg.	
	38 (##26)	HANDKEYS	
	39 (##27)	ERROR HANDLING OPTns. (DETAIL SECT.9)	
	40 (##28)	UPPER LIGHTS	
	41 (##29)	LOWER LIGHTS	
	42 (##2A)		
	43 (##2B)	IPL DATA	
	44 (##2C)	OPER LIGHTS SLAVE	
	45 (##2D)	PEI PARAM	
	46 (##2E)	W.S. IDENT.	
	47 (##2F)	SEI PARAM.	
	64((#40) - 71(=47)	1900 ACC's 0-7	1900 ONLY
	72 (#48)	FPACØ	1900 ONLY
	73 (#49)	FPAC1	1900 ONLY
	74 (#4A)	DATUM	1900 ONLY
	75 (#4B)	LIMIT	1900 ONLY
	76 (#4C)	SMO	1900 ONLY
	77 (#4D)	ESR	1900 ONLY
	78 (#4E)	MEB	1900 ONLY
	79 (#4F)	OBEY	1900 ONLY
	82 (#52)	TGT BLK ADD	
	94 (#5E)	LAST 7 BITS of PC,LOG POINTER	
	96 (#60-DF)	PC LOG AREA	

OPERATING INSTRUCTIONS FOR RUNNING T.C.S.S. UNDER EMAS.

HAVING LOGGED IN TO E.M.A.S. AS NORMAL PROCEED AS FOLLOWS :-

COMMAND: LTP XXXX WHERE XXXX IS THE 4 CHAR PROG. NAME.
(FOR THE FOLLOWING EXAMPLE WE SHALL ASSUME XXXX = EDA

TCSS 5.2

PLEASE SELECT UNIT FOR DEV0: YYYY WHERE YYYY = ALPHA NUMERIC MNEMONIC FOR 1ST DEVICE TO BE TESTED
SEE NOTE 1
AND NOTE 3

YYYY USED AS DEV0

PLEASE SELECT UNIT FOR DEV1: ZZZZ WHERE ZZZZ = ALPH NUMERIC MNEMONIC FOR 2ND DEVICE TO BE TESTED
SEE NOTE 1
AND NOTE 3

ZZZZ USED AS DEV1

PLEASE SELECT UNIT FOR DEV2: FORGO i.e. NO FURTHER TEST DEVICES

PROGRAM EDAR(1) LOADED SUCCESSFULLY

>- TCSS/TEST PROGRAM HAVE NOW BEEN ENTERED AND ALL STANDARD TOSD/TCSS COMMANDS, WITH THE EXCEPTION OF BREAKIN, ARE VALID. FOR BREAKIN SEE NOTE 2.
FOR LIST OF VALID COMMANDS SEE TCSS TPUM

>- LGT CAUSES TCSS/TEST PROGRAM TO BE DELETED AND PROCESS TO BE LOGGED OUT

NOTES ON RUNNING T.C.S.S. UNDER E.M.A.S.

1/ DEVICE MNEMONICS

AS T.C.SS / TEST PROGRAMS REQUIRE 4 CHAR MNEMONICS (NORMALLY TWO ALPHA FOLLOWED BY TWO NUMERIC CHARS) AND SOME EMAS MNEMONICS ARE ONLY THREE CHARS LONG CERTAIN GROUND RULES MUST BE OBSERVED. THESE RULES ARE AS FOLLOWS :-

i/ EDS MNEMONICS — USE EMAS MNEMONIC

ii/ M/T MNEMONICS — IF THE LEAST SIGNICANT DECK IS M10 THEN THE CONCEPTUAL EMAS CLUSTER MNEMONIC BECOMES MC10 FOR M20 THEN MC20 ETC.

iii/ SLOW DEVICE MNEMONICS — WHERE THERE ARE ONLY 3 CHARS IN THE EMAS MNEMONIC THEN A LEADING Ø IS PLACED BEFORE THE NUMERIC CHAR i.e.

CRØ BECOMES CRØØ
LP1 BECOMES LPØ1
LP11 REMAINS LP11

2/ BREAKIN

AS "CONTROL ∝ A" IS MEANINGLESS TO EMAS BREAKIN IS ACHIEVED BY HITTING "ESCAPE" ("CONTROL, SHIFT ∝ K" ON LIMITED SET T/T COMPATIBLE VDU'S) AND WHEN PROMPTED INT: REPLYING "BI". MULTIPLE BREAKINS ARE PERMISSABLE AND WILL CAUSE INSTANT BREAKIN TO TCSS WHEN THE TEST PROGRAM IS RUNNING.

3/ AVAILABILITY OF DEVICES FOR TESTING

BEFORE DEVICES CAN BE ACQUIRED BY TCSS FOR TESTING THEY MUST BE IN THE CORRECT SYSTEM STATE. THIS CAN BE ACHIEVED AS FOLLOWS :-

i/ E.D.S

IT IS SUFFICIENT TO MOUNT A NON-STANDARD DISC (i.e. EDAR DISC) ON THE DRIVE(S) TO BE TESTED.

ii/ M/T's

FOR M/T'S IT IS NECCESSARY TO TYPE THE FOLLOWING AT THE MAIN CONSOL

V/ MXX MODE = OFF

WHERE MXX IS [redacted] THE EMAS MNEMONIC FOR THE DEVICE. n.b. THIS MUST BE DONE FOR EVERY DECK IN THE CLUSTER TO BE TESTED.

iii/ SLOW DEVICES

FOR SLOW DEVICES IT IS NECCESSARY TO TYPE THE FOLLOWING AT THE MAIN CONSUL

S/ XXX LIMIT Ø

S/ ABORT XXX WHERE XXX IS THE EMAS MNEMONIC OF DEVICE TO BE TESTED.

SHOULD THE DEVICE(S) NOT BE IN THE REQUIRED STATE WHEN TCSS ATTEMPTS TO ACQUIRE IT THEN THE MAIN OPERATOR CONSUL WILL BE PROMPTED AS FOLLOWS :-

"PLEASE CONFIGURE OUT XXXX"

TWO COURSES OF ACTION MAY THEN BE TAKEN

i/ THE DEVICE CAN BE MADE AVAILABLE AND THE PROMPT ANSWERED "PDN" (PROMPT DONE), T.C.S.S WILL THE CARRY ON AS NORMAL.

ii/ THE PROMPT CAN BE ANSWERED "CD" (CANT DO). AN APPROPRIATE MESSAGE WILL BE OUTPUT AT THE TERMINAL AND TCSS & TEST PROC. WILL BE DELETED AND THE SESSION TERMINATED.

n.b. AS EMAS IS NOT BLOCK STRUCTURED RESOURCES ARE NOT

NECCESSARILY SURRENDERED AT THE END OF SESSION. THE TCSS-EMAS SUPPORT PACKAGE WILL, OF COURSE, RELINQUISH ALL DEVICES ALLOCATED TO IT AT THE END OF SESSION. THIS, HOWEVER, PRE-SUPPOSES A CLEAN EXIT FROM TCSS. A SITUATION CAN ARISE WHERE TCSS IS NOT EXITED FROM IN A TIDY MANNER e.g. IN THE EVENT OF A CRASH IN THE ENGINR. PROCESS DURING RUNNING OF TCSS/TEST PROGRAM. THIS CAN LEAD TO A SITUATION WHERE ENGINR "OWNS" A DEVICE(S) BUT T.C.SS/TEST PROGRAM CANNOT USE IT AS ANY ATTEMPT TO ALLOCATE IT FAILS AS IT IS ALREADY ALLOCATED. SHOULD TCSS/TEST PROGRAM CRASH DURING RUNNING IT IS ADVISED THAT ANY ALLOCATED DEVICES ARE MANUALLY RELEASED. TO THIS END A SPECIAL COMMAND "RELEASE" HAS BEEN PROVIDED. THIS TAKES THE FORM

COMMAND: RELEASE XXXX where XXXX IS THE EMAS MNEMONIC

IT IS FURTHER ADVISED THAT IN THE EVENT OF A CRASH NO ATTEMPT IS MADE TO RE-ENTER TCSS WITHOUT FIRST LOGING OUT AND LOGING IN AGAIN. IT WON'T WORK AS CERTAIN TCSS VARIABLES WILL NOT HAVE BEEN RE-INITIALISED.

GENERAL DESCRIPTION SRU

PART 'D' SECTION 1

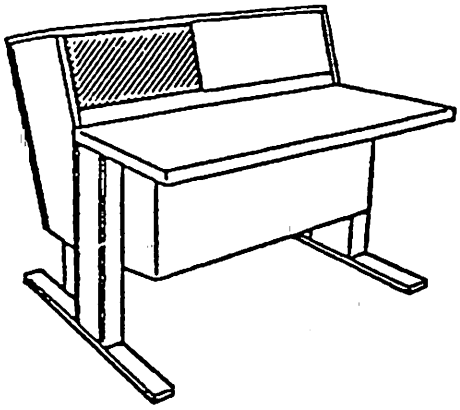
1.1 Major system units SMAC, SAC and OCP on a dual system are configured by the (SYSTEM RECONFIGURATION UNIT) SRU. System units SAC and OCP are visible to the system via the ports of SMAC. The SRU uses HI HO control over transmitters and receivers of the port interfaces, and also to isolate the (DIRECT WIRED INTERFACE) DWI. The DWI is an interface between SAC and OCP, OCP and OCP, in a dual configuration.

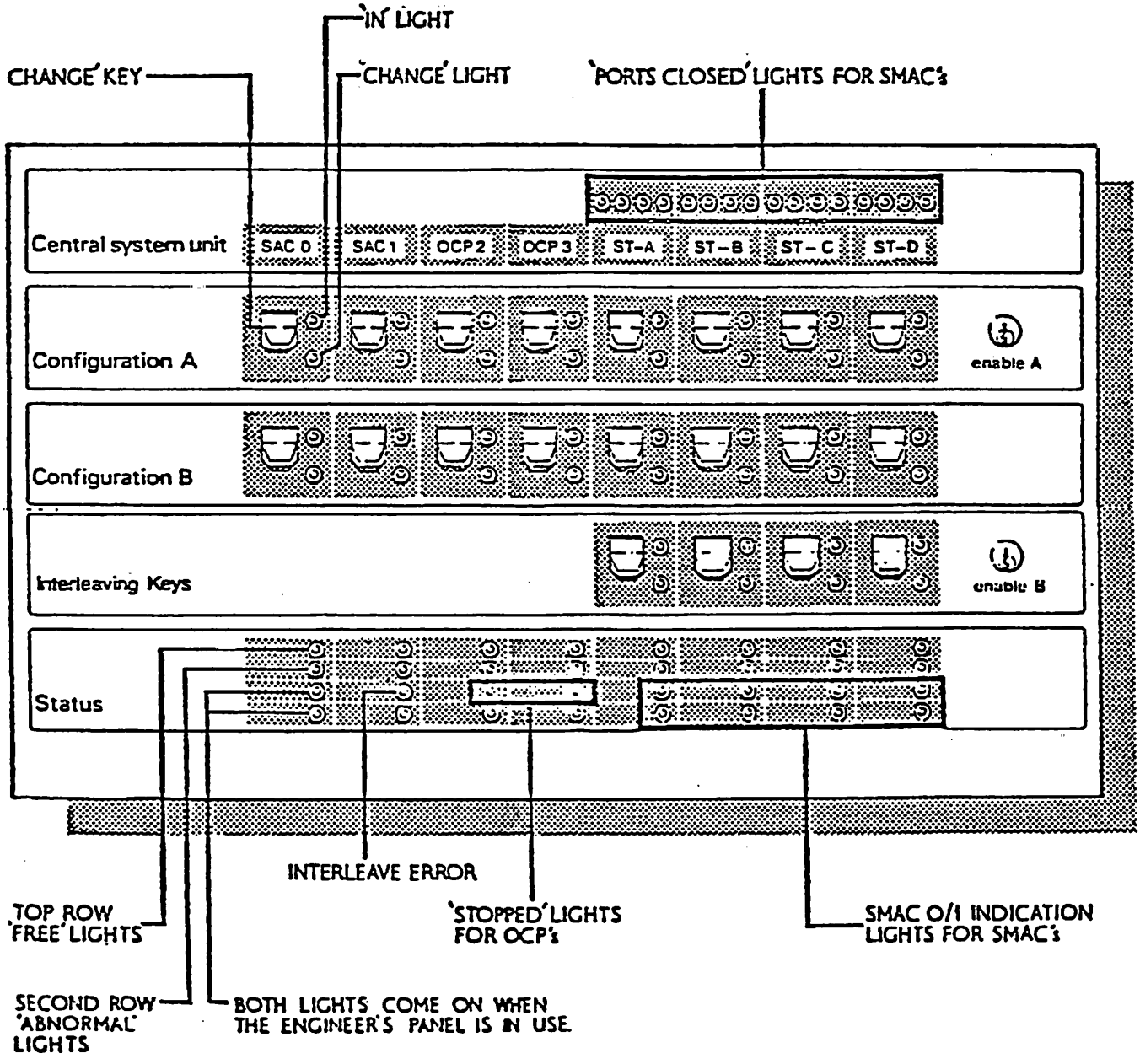
The configuration is set on the SRU at load time. Thereafter, the configuration is set by writing to an image store in SMAC to enable dynamic reconfiguration. This software can be envoked by the command (CONFIGURE DEVICE STATUS) CDS or by a software decision to remove a unit from the configuration if not being used.

1.2 The SRU

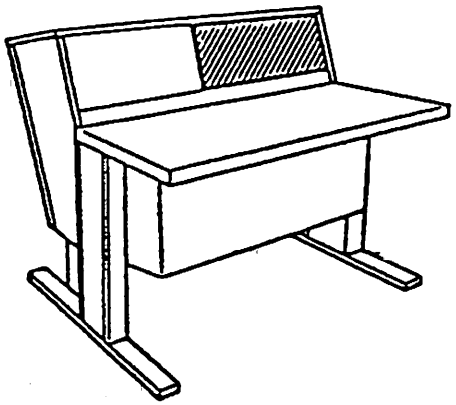
This unit has two main panels accessible to the operator. Both the panels are divided into two. The left hand panel is the reconfiguration panel. This panel has sixteen switches, eight in either half. The 2976 has an extra 4 switches, set below the standard sixteen switches. These are for interleaving configuration.
A dual configuration can be set in either half 'A' or 'B'. If a configuration is set in both 'A' and 'B', the system is said to be partitioned. In a dual configuration all units are set in one half. To set a configuration, all switches must be put down to the change position, this will illuminate the red change light below the switch. A change can only take place if the unit is in the free state, this is indicated by a green light at the bottom of the panel. A unit is set into a configuration by the operation of the appropriate enable key 'A' or 'B'. All keys selected to the change state must be put to the normal position (up), because if the enable key for that configuration is pressed again with the key in the change position, it will be removed from the system and become free.

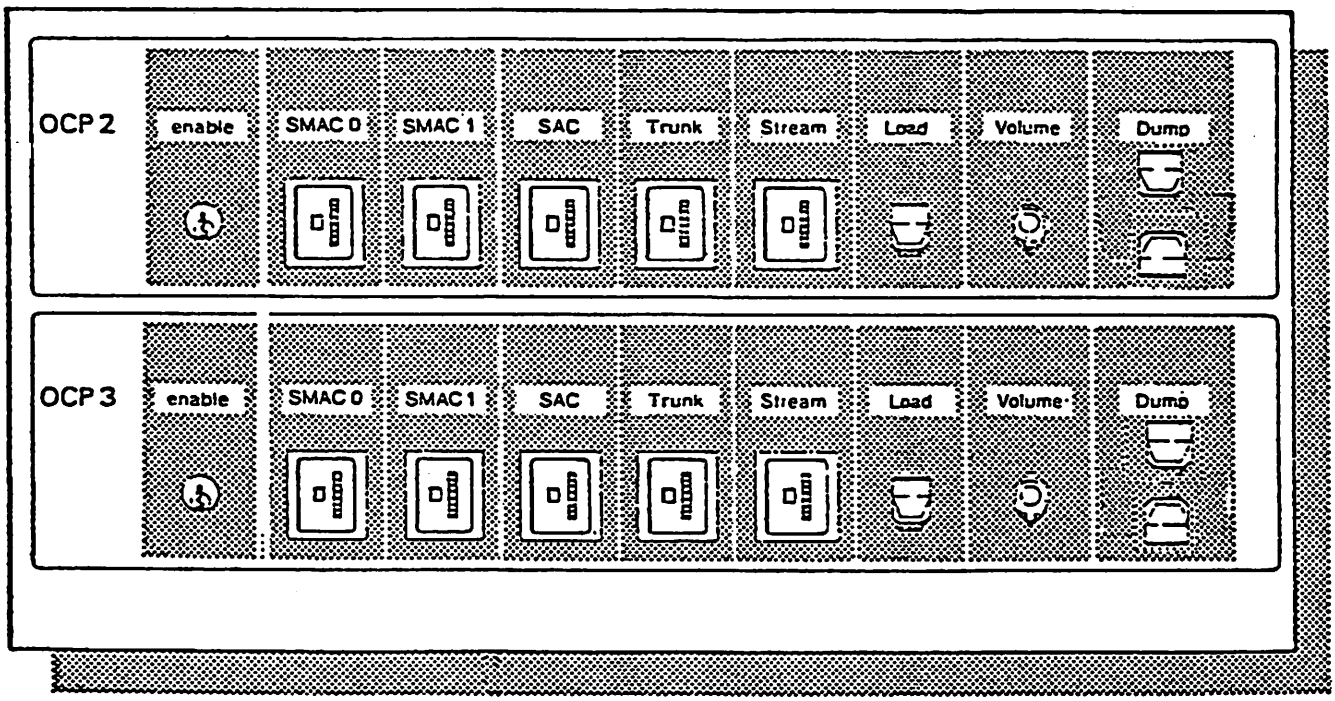
Other indicators on this panel are port closed lights which are positioned above the SMAC switches. These indicate when SMAC ports are closed. Along the bottom of the panel there are four rows of indicator lights. The top row of these indicate when the unit directly above it is in a 'free' state i.e. not in either configuration. The second row indicate an abnormal condition on the unit, this can be a power supply fail or an engineers switch left in an operative state. The third and fourth rows are not symmetrical and therefore will be described individually. The two lights at the left hand end indicate when lit that the engineers panel is connected to the SRU.





2976 RECONFIGURATION PANEL





2976/80 BOOTSTRAP PANEL

The operation of the engineers panel will be dealt with in a separate section. The next indicator on the third row is only fitted to 2976 SRUs and indicates an interleaving error. This condition will occur when the interleaving rules are broken. The next set of lights are in the third row below the OCP change switches and indicate when the OCP is in the stopped state. The last set of lights are a group of four and relate to the SMAC number. The 2976 differs in this respect to all other 2900's the SMAC number here is always in pairs module 8 apart.

1.3 Bootstrap Panels

The bootstrap panels are situated on the right hand side of the SRU. These two panels are divided in two halves - one for OCP2, the other for OCP3. Each half contains thumb wheels to select the IPL path, a volume control and switches for load and dump. The panels vary in layout within the 2900 range. 2980 and 2976 have an extra thumb wheel switch, as these machines have the facility to interleave.

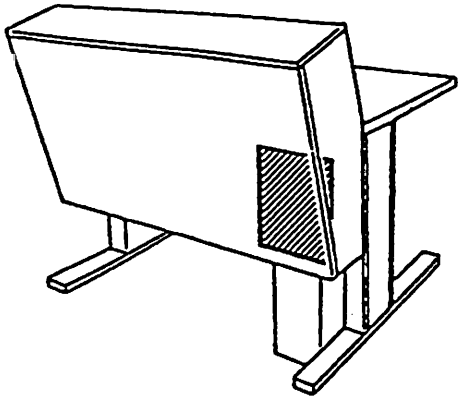
The operation of this panel is reasonably self-evident. The SMAC or SMAC's and SAC numbers are selected on the thumbwheels the SMAC number is in the range A to D. This letter relates to the ST letter selected on the reconfiguration panel. The letter selected will deem that SMAC to be SMAC Ø. The SAC number is in the range 0 to 1 as only two SAC are allowed on the system. The other two thumb wheels select the trunk and stream of the IPL path, both in the range 0 to F. When the selection is complete, the load or dump keys are operated simultaneously with the enable key. Note there are two dump keys for each panel which must be operated at the same time to envoke the dump sequence.

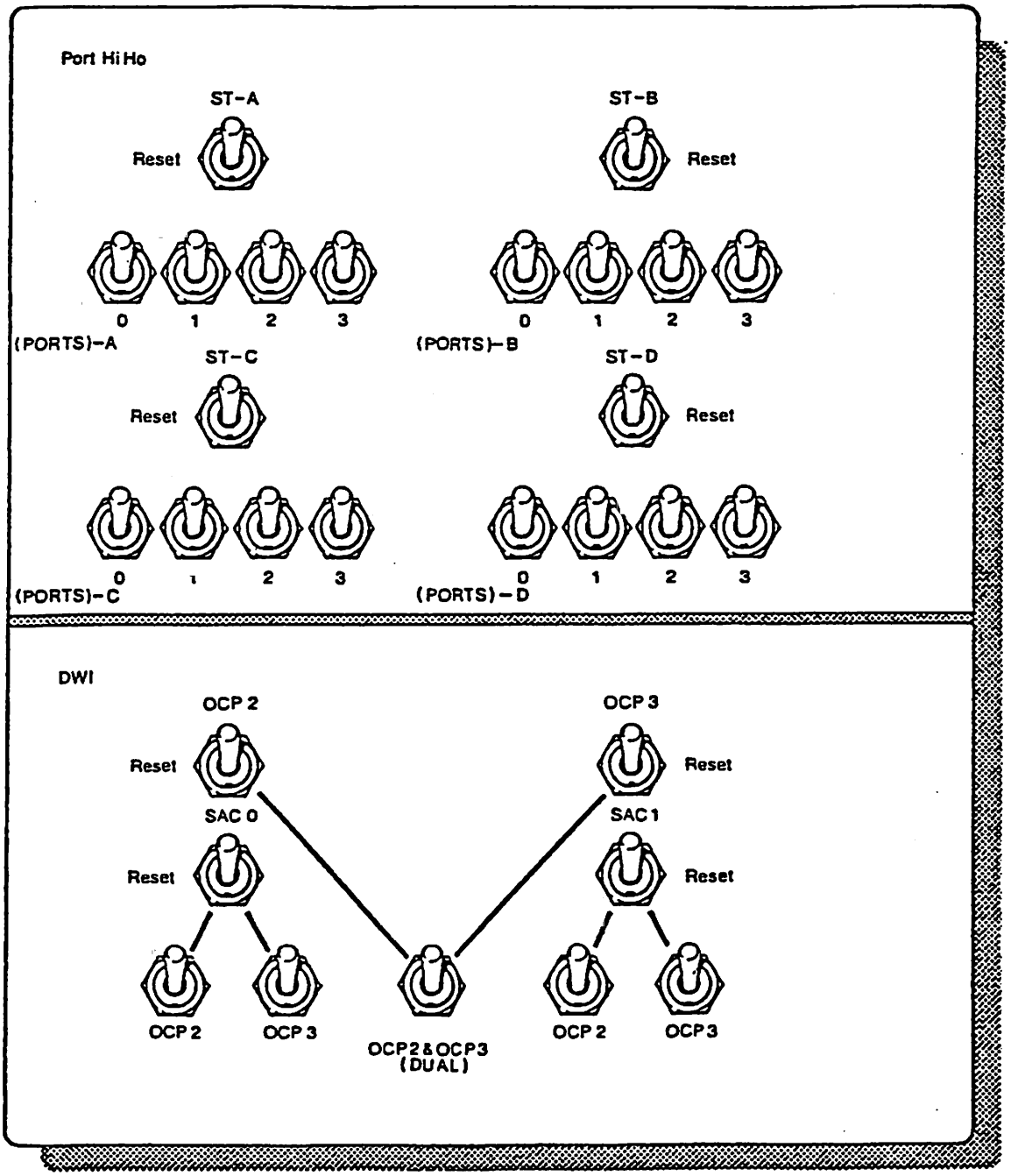
1.4 Engineers Panel

This panel is situated at the rear of the SRU behind the rear cover. Normally the connecting cables 1R and 2R will not be connected. As stated in section 1.2, when this connection is made a two-light display will illuminate on the operators reconfiguration panel. The purpose of the engineers switch panel is if the power supply fails in the SRU, a configuration can be set on the engineers switches to simulate the original configuration to enable the customer to continue.

1.5 Engineers Panel Operation

The switches on this panel are operative when in the (up) position. There are twenty one toggle switches and eight bias switches. The panel is divided into two halves, the upper half is port control, the lower is DWI control. To set a dual configuration using two SMACs, two SACs and two OCPs, put all toggle switches 0, 1, 2, 3 up on port 'A' and 'B'. Put the lower five toggle switches up. Operate the bias switches for port 'A' and 'B'. Operate the bias switches on the DWI half for OCP2, OCP3, SAC Ø and SAC1. The bias switches produce local IPL signals and open the path for the IPL. Complete system load as per section 2.4, 3.4 4.7 for 2960, 2970 and 2976 respectively.





ENGINEERS PANEL

NOTE: THE POSITION OF THE KEYS SHOWN IN THIS FIGURE IS THE 'OPERATIVE' POSITION

To partition neatly in two balanced halves using one SMAC in each half, set the switches as follows :

Port 'A' switches - Put switches 0 and 2 to 'up' and switches 1 and 3 to 'down'.

Port 'B' switches - Put switches 1 and 3 to 'up' and switches 0 and 2 to 'down'.

DWI half left hand switches set, OCP2 switch 'up' OCP3 switch 'down'.
Right hand switches set OCP3 switch 'up' OCP2 switch 'down'.
Set centre toggle switch 'down' this will break the DWI interface between OCPs.
Operate bias switches for Port 'A', port 'B', OCP2, OCP3, SAC Ø and SAC 1. This action will produce local IPL and set the port paths for IPL.
Complete the system, load as per sections 2.4, 3.4 and 4.7 for both OCPs.

Alternative Partition

To set a partition using SMAC 'A' SAC1 and OCP2 in one half, and SMAC 'B' SAC Ø and OCP3 in the other half.

Port 'A' switches, set switches 1 & 2 to 'up', set switches Ø and 2 'down'.
Port 'B', set switches Ø and 3 to 'up', set switches 1 & 2 'down'.

DWI switches, left hand switches, set toggle switch OCP3 to 'up', set toggle, switch OCP2 to 'down'.

Right handswitches set toggle switch OCP2 to 'up', set toggle switch OCP3 to 'down'

Operate the bias switches for Port 'A', Port 'B', OCP2, OCP3, SACØ and SAC1, this action will produce local IPL and set the port paths for IPL.

Complete the system load as per sections 2.4, 3.4 and 4.7 for both OCPs.

Interleaving Switches (2976 only)

1.6 There are four interleave switches one for each store. To select stores for interleaving, the switches must be put down to the change position. Also, the associated SMAC switch must be put to the change state. Interleave switches and SMAC switches must be selected in pairs, the following are allowed :

A&B, A&D, C&D, B&C.

Any other combination of pairs will result in the 'error' light being illuminated. When the switches are selected to the change state, the enable key A or B to which they are to be configured is pressed. If the action is successful, the 'IN' light will be illuminated for each change.

S.R.U.

1.7. GENERAL DESCRIPTION APPENDIX FOR 2976 S.R.U.

BOOTSTRAP PANEL

On this panel there are two 'force SMAC' thumbwheels for each OCP row, namely SMAC 0 and SMAC 1.

The 'force SMAC 1' thumbwheel also has a blank position to accommodate the need for not having a SMAC 1. These thumbwheels are to conveniently facilitate a four SMAC interleaved system.

Certain numbering restrictions are imposed when interleaving in addition to the physical restrictions mentioned in section 1 - 6:- ST A and ST C are termed the even SMACs, ST B and ST D are termed the odd SMACs.

The convenient valid states are:-

SMACs Interleaved	SMAC NOs
A and B	0 and 8 or 1 and 9
C and D	0 and 8 or 1 and 9
B and C	8 and 0 or 9 and 1
D and A	8 and 0 or 9 and 1

It can be seen from the above table that:-

1) You cannot interleave 2 even SMACs
2) You cannot interleave 2 odd SMACs
3) The even SMAC must have the lowest number

On a duals site all of the above options cannot be used without altering the SMACs natural number.

For a four SMAC interleaved configuration it is usual for the SMACs to have the following addresses, but not obligitory.

ST		NATURAL No
SMAC A	=	A
SMAC B	=	8
SMAC C	=	B
SMAC D	=	9

All 4 SMACs interleaved Force 0 = A or C

Force 1 = C or A

It can be seen from this numbering system that if you partition, in two balanced halves, only one configuration can be interleaved, i.e. whichever configuration has SMAC 'D', with natural number of 9, cannot be interleaved, the reason being that you must have a SMAC 0.

On a 2976 SRU the SAC thumbwheel has a blank position. This thumbwheel is used to allow the SAC activate and the SAC interrupt in the IPL OCP. When doing an IPL in a dual configuration with two SACs and two OCPs, the non-IPL OCPs associated SAC thumbwheel must be set to blank. This puts the non-IPL OCP into a suspended state.

SRU CONFIGURATION TECHNICAL OPERATION

1.8. General

When the SRU is switched on, all logic is held in a 'frozen' state, a mechanical timer is situated at the rear of the unit. The timer is adjustable from 0 - 60 seconds, and should be set to 15 seconds.

A configuration is set by putting the appropriate change switches down. The action can only successfully be completed if the unit to be changed is in the 'FREE' state. The action of the change switch is to prime a binary, the setting of binary is clocked by clock pulse 2 when the reconfiguration enable key is operated.

The enable key produces two clock pulses, clock 1 and clock 2. Clock 1 is a 5ms pulse separated from clock 2 by 5ms. Clock 2 is a 30ms pulse. Clock 1 sends a local IPL signal to the SMAC, this will set an OCP port to 'OPEN'. The SAC ports are not established until clock 2 time, and are set in the SMAC at bootstrap load time.

Clock 2 sets the configuration selected into the logic, where it is locked into binaries and then via gating control operate logic relays. The relays control the HI HO lines of each units connected interface, this also includes the direct wired interface.

1.9. Engineers Switches

As can be seen by the accompanied logic drawings, the engineers switches sit across the relay outputs. Thus in the event of a power failure, the selected configuration can be simulated (see general SRU description). It is also evident from the drawings that the engineers switches must not be left in an operative position, as they override the relays if the engineers panel connecting plugs are left unconnected, this condition will be indicated by two leds on the reconfiguration panel.

1.10. Interleaving Configuration

The logic employed is designed to make certain the rules for interleaving are obeyed (see Table 1). If the rules are broken, then an error signal will be produced, and an indication of this shown on the operators reconfiguration panel. If allowed pairs are selected, this will operate the appropriate relays to signal to the OCP and SAC, to treat that pair as interleaved store.

TABLE 1

	STA	STB	STC	STD
allowed interleaved pairs	✓	✓		
	✓			✓
			✓	✓
		✓	✓	

PART D SECTION 2

DUALS COMMISSIONING

2.1.0 This document assumes that the system reconfiguration unit (SRU) has been physically installed.

2.2.0 Relevent Documentation

SRU Technical Description 65/94682
SRU Installation Description 65/94690
TPUD Part B Volume 1 (Test Program IPCT, Dual)
TPUD Part B Volume 3 (Test Program NF 2960)

2.3.0 SRU Static Checks

3.1 Check the following areas and observe that no damage has occurred during transit.
3.1.1 All covers fit and operate correctly and are not damaged
3.1.2 That all connectors, plugs, sockets, etc. are fitted and located correctly.
3.1.3 All package pieces have been removed as per installation data Document No. 65/94690.

2.4.0 Power Supplies

4.1 Warning hazardous energy.
4.1.1 Check mains switch is off
4.1.2 Carry out check for short circuit on IAMDA + 5 volt power supply.
4.1.3 Using a DVM set to OHMS scale, with 0.5 range selected measure resistance across TBI and TB2 located behind lower front cover reading should be approximately : 5 OHMS

2.5.0 Switch on Mains switch located at rear of unit.

5.1 Using a DVM set volt range check between TBI and TB2 for + 5 volt ± %5 if this is not present adjust power supply by means of potentiometer located at the right side of the LAMDA power supply.

2.6.0 Configuration Mode checks

6.1 With power applied to the unit and all switches in the up position, check that all the 8 (Free) lights are illuminated.
6.1.1 Switch all 16 selection switches down and press (A) enable key once. Observe that all 8 (IN) lights are illuminated. Press enable (B) key once and observe there is no change in the configuration.

2.6. continued

6.1.2. Press enable A key once and observe all 8 (Free) lights are illuminated and all 8 configuration (A) (IN) lights are extinguished. Press enable (B) key once and observe all 8 (Free) lights are extinguished and all 8 configuration (B) (IN) lights are illuminated. Press enable (A) key and observe there is no change in the configuration. Press enable (B) key once and observe that all 8 configuration (B) (IN) lights are extinguished.

2.7.0. PARTITIONED SYSTEMS

Set switches on SRU reconfiguration panel for system (A) as in table (1) column (A). Press enable key once. Set switches on SRU reconfiguration panel for system (B) as in table (1) column (B). Press enable key once. Set OCP 2 section of bootstrap panel to Port Trunk and Stream of the media selected for system load. Press the associated load switch and enable key on bootstrap panel simultaneously. Repeat the above procedure for system (B) and OCP 3 section of bootstrap panel.

2.7.1. Repeat 7.0. procedure for columns (C) and (D) table(1).

2.8.0. Set switches on SRU for system as in table (1) column (E). Press enable key once. Set OCP 2 section of the bootstrap panel to Port Trunk and Stream of media selected for system load.

2.8.1. Load and run free standing test "IPTC" TPUD Part A Volume (1) when complete, load and run free standing test 'Dual'.

2.8.2. Repeat the above procedure using OCP 3 section of bootstrap panel using table (1) column (F).

TABLE 1	A	B	C	D	E	F	G
SAC 0	IN			IN	IN	IN	IN
SAC 1		IN	IN		IN	IN	IN
OCP 2	IN			IN	IN	IN	IN
OCP 3		IN	IN		IN	IN	IN
ST -A	IN			IN	IN	IN	IN
ST -B		IN	IN		IN	IN	IN
ST -C	(IN)			(IN)	(IN)	(IN)	(IN)
ST -D		(IN)	(IN)				(IN)

ST -C fitted only to 2970 and 2976/80 systems

ST -D fitted only to 2976/80 systems

2.9. DUALS COMMISSIONING S.R.U. APPENDIX 2976

Set switches on SRU for system (A) as in table (1) column (G) with the SMACs non-interleaved. Press enable key once. Ensure the SMACs are not forced to 0 or 1 using the SMAC engineers panel. Set, on OCP 2 section of bootstrap panel, SMAC 0 thumbwheel to A and SMAC 1 thumbwheel to B. Press associated enable key and load switch on bootstrap panel simultaneously. Check that the SMAC 0/1 indicators on the reconfiguration panel are lit accordingly. Repeat the above procedure checking that each SMAC can be forced to 0 and 1. Repeat the procedure for OCP 3 section of bootstrap panel.

N.B. A reset from the OCP with the undump key in the down position will cause the SMACs to revert to their natural numbers.

2.9.1. Check that any illegal interleave conditions (see general description section 1.6.) lights the "Interleave Error" L.E.D. on the reconfiguration panel.

2.9.2. Set up switches on SRU for system (A) as in table (1) column (G) with all four SMACs interleaved (see SRU general description section 1.6.). Press enable key once. Assuming SMAC natural numbers are set to:-

SMAC A = A

SMAC B = 8

SMAC C = B

SMAC D = 9 then set, on OCP 2 section of bootstrap panel SMAC 0 thumbwheel to A and SMAC 1 thumbwheel to C. Press enable key and load switch simultaneously. Using OCP engineers panel, check that the stores can be written to and read from, and that the 'interleaved STATS' are set (STIF Frame 6 Line 9 bits 32-35). There is no visible indication of interleaving in the SACs, therefore, using a scope, check the interleaving signals in both SACs. (SAC 3A/3B ED's Page 14.7 Pins AM 2L, AM 1R, AM 3L and AM 3R).

2.9.3. Set switches on SRU for system (A) as in table (1) column (G). Press enable key once. Set OCP 2 section of bootstrap panel to Port, Trunk and Stream of media selected for system load. Set SAC thumbwheel on OCP 3 section (non-IPL OCP) to blank. Press enable key and load switch simultaneously. Check that the non-IPL OCP (i.e. OCP 3) goes to a suspended state, i.e. COM 8 (frame 10 Line 8 bit 10). Repeat the above procedure using OCP 3 section for the selected media address and setting SAC thumbwheel to blank on OCP 2 section.

2.10. ENGINEERS SWITCHES SRU

2.10.1. To Partition System

Port H1 HO Switches

Switch ST-A switch 0 & 2 up. Operate ST-A reset switch

Switch ST-B switch 1 & 3 up. Operate ST-B reset switch

Left-Hand Switches (LOWER)

Switch OCP2 switch up switch OCP3 switch down, operate SACØ reset switch

Right-Hand Switches (LOWER)

Switch OCP3 switch up switch OCP2 switch down, operate SAC1 reset switch

Carry out IPL sequence from OCP engineers panel (2970) ECP (2960)

When load sequence is complete, check that selected ports are indicated on the SRU front panel leds.

2.10.2. To Dual System

Port H1 HO switches

Set all port switches of operational SMACs to up, activate all operational ST reset switches.

DWI switches

Set lower 5 switches to up, activate all reset switches OCP2, SACØ OCP3, SAC1.

Carry out IPL sequence from OCP engineers panel (2970) ECP (2960)

When load sequence is complete, check that selected ports are indicated on the SRU front panel leds.

- SMAC Ports and numbers must be forced at the SMAC's and the OCP Engineers facilities used to 'IPL'.

Section 2.2. Creating a u code dump tape

	STEP	
ECP	1.	Type FI UTIL SICL 'SEND' and await flashing cursor
	2.	Unload TLOE cassette by depressing → and CNTRL keys together and replace with u code cassette.
	3.	Type SICL and 'SEND' and await completion of u code load to main store.
	4.	Type WWS 2B 2000 0000.
	5.	Unload u code cassette using → and CNTRL keys and replace with TLOE cassette.
M.T.	6.	Load a working tape on to lowest order deck on M/T cluster.
ECP	7.	Type DU pts 'SEND'

Port trunk and Stream of M/T unit

u code will now be dumped to working tape.

8. Repeat action 7 several times to reserve further copies of u code on the tape.

A. TCSS FACILITIES

See Appendix A for list of available test programs.

TCSS COMMANDS

LOAD_TEST_PROGRAM (LTP)	This macro establishes the environments for engineers test programs

PARAMETERS

MODULE = NAME OF TEST PROGRAM FILE
ASSIGNMENT = DEVICE/LINE/CONTROLLER MNEMONIC
ACTUAL UNITS = DEVICE MNEMONIC
EXTEND = LIBRARY NAME
ROUTE = SPOOLED/ONLINE
RESPONSE = RESULT)

ABANDON(ABA)	Abandons test program selection at earliest opportunity
ABORT(ABO)	Abandons current selection immediately
ATERROR_DEFAULT(ATEDEF)	Returns default option to calls from test program
ATERROR_RECOVER(ATEREC)	Returns recover option to calls from test program
ATERROR_ASK(ATEASK)	Removes the other two aterror conditions
CYCLE(CYC)	Causes a selection to be cycled
CYCLE_OFF	Cancels the cycle command
GO	Starts off test program selection
HOLD(HOL)	Causes a repeat option to be returned to test program
HOLD_OFF(HOLOFF)	Cancels the hold action
LOCK(LOC)	Causes repeat options to be returned to test program until a different h/w error occurs, the h/w operation is successful or the program is unable to repeat the operation.
LOCK_OFF	Cancels the lock action

ON_TP	Sets bits in test options word Eg, ON_TP ("3 5 9")
OFF_TP	Resets bits in test options word
RECOVER(REC)	When RECOVER option offered causes test program to perform defined recovery action
REPORT(REP)	When REPEAT option is offered causes the test program to repeat the failing operation
ROUTE(ROU)	Causes messages of the specified class of set of classes to be routed as instructed. Eg, ROU("20 BULK")
SELECT(SEL)	Causes an element to be selected. Activated by GO command. EG, SEL(ALL)
SET	Enables the setting of test parameters declared by the test program. Eg, SET UTIL = "E"
SELECTANDGO(SGO)	Equivalent to SELECT command followed by GO, eg SGO(ALL)
STEP(STE)	Executes the current selection one element at a time and halts at the end of each element
STEP_OFF	Cancels the STEP action
SUSPEND(SUS)	Suspends the test program until a GO command is issued
TERMINATE(TER)	Causes termination of the current element at the earliest possible opportunity but allows the rest of the selection to continue
WHATIS(WHA)	Puts on the oper details of the following: PARAMETERS ELEMENTS PARAMETER NAME TESTOPT

EXAMPLES OF RUNNING TCSS

TCSS tests with standard set of node calls can be run from oper by typing:

ET(TESTNAME)

The test units, which must be configured out, will be prompted for. Alternatively for a wider selection of required nodes the test can be input as a job as shown below:-

```
CUJ(:ENGINEER)
J(EDAR)
BEGIN
LTP(EDAR)              @will prompt for test unit, which must be
SET UTIL = "E"          configured OUT.@
SGO 99.8
SET UTIL = "N"
SGO 3
ABA
END
ENDJOB
****
```

Can also be run in MAC environment

The engineers OCF (S ENG or S 12) can be displayed for information on progress of a test.

4. DUAL SYSTEM ERRORS

4.1 Failing OCP

(a) 2960/2970

For any system error other than a timeout resulting from an access to the other OCP, the failing OCP will broadcast the fact that it has had a system error, and then 'go to sleep'. In the case of a timeout, the system error is not broadcast, as the remote OCP is presumed to be dead.

'Sleep' involves looping in the microprogram at the following addresses:-

2970	19I5	771 - 772
	7000	77B - 77C
	1000	783 - 784
2960	C14	1037 - 103E
	C17	10CC - 10D3

The microprogram will remain in this loop until a Block 2 Subblock 60/63 image store access is performed from the other OCP with Bit 12 = 0, i.e. do not suspend on completion. On 2970, the EKS key may be used to get out of this loop manually. On 2960, typing HA will take it to 'Tidystop'.

(b) 2976 Types

The following types of system error are broadcast:-

Irrecoverable H/W SEs, including failing retry.
Masked S/W SEs, i.e. SEI is masked in SSR.
This is only when SEI Analyser is runni_.

SGSE (FSEI)

For other crash conditions, e.g. MVSI or MPE, SEI-Analyser is entered in the detecting OCP, and will suspend the other OCP by accessing IS 42PØØØØ4. Note that this does not cause an SSN+1 dump, so PC, LNB etc, can only be obtained from the lights. The 'suspend' condition is shown by COMM8=1 (Frame 10, line 8, bit 10).

On receipt of a broadcast SEI, the H/W 'Masks' MULT until the SEI parameter has been read from the failing OCP, at which point it is 'unmasked', and any further SEIs will be broadcast back to the failing OCP. SEI-Analyser therefore unsets MULT before reading the parameter.

Timeout system errors resulting from remote OCP or SAC accesses are not broadcast.

4.11 HARDWARE SYSTEM ERROR PARAMETER - 2960

System Error

Hardware System Error	(32 bit word)
Bits 0 - 2	Failing Module No. If the system error is reported in a processor other than the originating module, i.e. if bits 0-2 of the parameter are not equal to the module number of the reporting processor, bits 3-31 of the parameter are zero.
Bits 3, 4	01 Irrecoverable Error 10 Successful Retry 11 Retry Failed (Code 00 used for Software System Error)
Bits 5 - 7	Zero
Bits 8 - 11	ACR
Bit 12	Zero
Bit 13	0 Photograph taken 1 No Photograph
Bit 14	0 SSN+1 OCP Register Dump 1 No SSN+1 Dump
Bit 15	0 Full Photograph)valid only 1 Mini only)if bit 13 = 0
Bits 16 - 31	Signify the failing Sub-Module (if bits 3, 4 ≠ 0, 0)
Bit 16	SMAC system error including Multibit Hamming failure
Bit 17	Single bit (recovered) Hamming failure.
Bit 18	Decoder Parity Error
Bit 19	SAU Parity Error
Bit 20	Store time out
Bit 21	OCP Internal time out
Bit 22	Microprogram Engine Parity
Bit 23	Data Parity Error from SMAC
Bit 24	Microprogram detected error
Bits 25 - 31	

Other bits to be defined for internal OCP-detected failure Bits 16, 17 and 20 are used for the same purpose on 2970.

4.12 SOFTWARE SYSTEM ERROR PARAMETER - 2960

(32 bit word)

Bits 0 - 2	Module Detecting failure
Bits 3, 4	0, 0 Software System Error
Bits 5 - 7	Zero
Bits 8 - 11	ACR
Bits 12 - 15	Zero
Bit 16	Illegal Virtual Store condition
Bit 17	Class 5 Interrupt Masked (VSI)
Bit 18	Class 7 Interrupt Masked (PEI)
Bit 19	Class 8 Interrupt Masked (System Call)
Bit 20	Class 9 Interrupt Masked (Out)
Bit 21	Class 10 Interrupt Masked (Extra code)
Bit 22	Stack Segment Number is ODD
Bit 23	Segment Table Format Error
Bit 24	Entry Forced by Software (Image Store)
Bit 25	ACS = Ø on Initial Activate
Bits 26 - 31	-

N.B. 4014000F indicates a forced dump.

5.4.3 cont. 2976 types: Set FSEI (Frame 1, Row 3, Bit 17) using the 'continuous set' key. This causes an SGSE to be broadcast. Either OCP may be used.

6. IMAGE STORE

This section explains how and when VME/B manipulates the more important image store locations when configuring IN/OFF an OCP.

6.1 Image Store Format (2960/2970)

0 2	3 31
BLOCK NO	FORMAT IS BLOCK DEPENDENT

If bits 0 - 2 = 0 the the IS access is to this OCP

If bits 0 - 2 = 2 then the IS access can be to this OCP or any other Port.

If bits 0 - 2 in the image store address decode to 2 then the following address format applies for OCP registers. (For a full explanation see PSD 4.2.3G).

0 3	4 7	8 11	12 15	16 31
0 1 0 0	0 0 1 0	PORT	NOTE A	CPU REGISTER ADDRESS

N.B. 1 Bits 5 & 7 are undefined but are invariably zero.

N.B. 2 Bits 0 - 3 are altered by the CPU hardware before being passed on to the external destination.

PORT This is the port to which the IS Command is to be sent.

NOTE A Bits 12 - 15 are used as follows:

Bit 12 = 0 Do not suspend OCP on completion of IS Command

= 1 Suspend OCP on completion of IS Command (OCP commonly referred to as asleep).

Bit 13 - 0 Then bits 14 and 15 are ingnored.

= 1 Interrupt as follows:

6.1 cont

Bit 14 - 0 Cause MPI on completion of IS Command

= 1 Cause SEI on completion of IS Command

Bit 15 This bit defines where the MPI/SEI caused by Bit 14 is to be sent.

= 0 The interrupt is sent to the port other than the one specified in the IS Command and it is generated as if it is an External Interrupt, i.e. an IS location must be read to clear it.

= 1 The interrupt is sent to the port specified in the IS Command and it is generated as if it is an Internal Interrupt, i.e. entering the software interrupt procedure via the IST clears the interrupt.

N.B. Bits 14 and 15 determine the type and destination of interrupt to be generated after the IS access to the specified address has been completed.

6.2 CPU REGISTERS (2960/2970)

6.2.1 6009 BROADCAST SYSTEM ERROR

This register controls whether System Errors are to be broadcast to the other OCP or not.

Bit 31 = 1 Broadcast SE
= 0 Don't broadcast SE

In normal dual running Bit 31 is set in both OCPs so that when either OCP SE's it is broadcast to the other OCP. On receipt of a SE from the other OCP bit 31 of 6009 (in the OCP handling the system error) is cleared by hardware. Bit 31 can be reset by software after SEI-ANALYSER has decided whether it is going to carry on using the failing OCP.

Broadcast System Errors is turned on in the OCP being configured in by KRM-DUAL-OCP-TEST and in the other OCP by KRM-CONFIGURE-IN-OCP.

It is turned off either by hardware or KRM-CONFIGURE--OFF-OCP.

6.2.2 600A SYSTEM INTERRUPT MASK

This register controls communications between port connected devices.

Bits 24 - 27 = SA (ACTIVATES) = MBI bits 8-11 on 2960
28 - 31 = SI (INTERRUPTS) = MBI bits 12-15 on 2960

Bits 24 & 28 Control Port 0
25 & 29 Control Port 1 etc.

If a bit is set in SA then it inhibits activates being sent to that port.

If a bit is set in SI it inhibits interrupts from that port.

On a dual system the following applies: the IPL OCP can receive interrupts from and send activates to all ports, the non IPL OCP cannot receive interrupts from the SAC(s) on the system but can send activates to all ports. The reason the non-IPL OCP is closed to the SAC(s) is so that on peripheral interrupts both OCPs don't go for the PERM CPU SEMAPHORE resulting in one OCP servicing the interrupt and the other looping on the semaphore (when the looping OCP gets the semaphore it would fall through PERM-SERVICE-RESPONSE as the interrupt has been serviced).

The bit settings of SA/SI corresponding to the port number of this OCP are ignored.

i.e. for port 3 bits 27 & 31 are irrelevant
port 2 bits 26 & 30 are irrelevant

6.2.3 6012 LOAD MICROPROGRAM

This register controls loading the microprogram to the OCP being configured in. KRM-CONFIGURE-IN-OCP calls KRM-GIVE-MICROPROGRAM to get the OCP microprogram and place it in SMAC Ø BLOCK Ø. Whilst the OCP microprogram is in block Ø photographs are inhibited by writing to IS 6011.

6.2.4 6302 SYSTEM ERROR INTERRUPT

This register is read by SEI ANALYSER (in the OCP that had a SE) in order to clear down the SE.

When KRM-DUAL-OCP-TEST is running in the OCP being configured in it reads this register so that the OCP is not declared to the system with a system error pending.

6.2.5 6303 MULTIPROCESSOR INTERRUPT

This register is read by KRM-HANDLE-MPI or VMM-MULTI-OCP-INT-HANDLER to clear down MPI's generated on successful Configure-In or Process-Reschedule respectively.

6.2.6 2960 M.B.I. (w.s. = 16)

0	EVENT PEND
1	
2	
3	
4-5	1900 DEC.SLOT.No.
6-7	S4 DEC.SLOT No.
8-11	SI MASK INHIBIT PORTS 0-3 TX Activate
12-15	SI MASK INHIBIT PORTS 0-3 RX Interrupts
16	JUMP CONDITION TRUE
17	DO NOT USE µ-PROG SYS.CALL CODE.
20	IST ACCESS
21	APSTB (WD's 0,1 SMAC 1)
22	SSN+1 DUMP
23	BROADCAST SEI
24	MPI
25	SEI
26	EXIS
27	COMMUNICATION SMAC No.
28-29	CLOCK MODULE No.

6.3 2976 Types OCP Image Store

6.3.1 4012 - S1

Bits Ø to 3		Allow external interrupts from modules Ø to 3, e.g. Real Time Clock (See note 2)
4 to 5		ACK/NACK Synchronisation Stats.
6	PS2U	Alternative PSTB in use. Set when PSTB has been loaded from the alternative area in SMAC 1.
7	IPHOT	Inhibit Photodump.
8 to 11		Hardware use. See Note 1.
12 & 13		Unused.
14, 15		Inhibit inter-OCP communication from Modules 2 and 3 i.e. Allow activates when set to '0'. This is to allow communication (e.g. Remote IPL) to to an OCP in the reset state.
16 to 19		Allow system error interrupts from Modules Ø to 3. See Note 2.
22	MPIS	Cause multiprocessor interrupt to self.
23	MPIX	Cause multiprocessor interrupt to other OCP .
24	DUAL	OCP is capable of being dualled. Setting bit has no effect on OCP without DUAL mods.
25	FMDU	FMDU & MLIB fitted. This bit may be reset by software to inhibit iterative divide. Setting the bit has no effect on an OCP without FMDU.
26 to 29		Allow Multiprocessor and Peripheral interrupts from Modules Ø to 3. See Note 2.

N.B. Except for bits 14 and 15, Ø = inhibit and 1 =allow.

6.3.2 4013 - S2

Bits Ø to 7		Unused. See Note 1.
8 to 11		Real Time Clock module number. See Note 3.
12	NONOV	Non-Overlapped.

6.3.2 cont.

Bits	13 INHERET	Inhibit retry.
	14 INHWBD	Inhibit wait before dump.
	15 PS2A	Set by software to indicate that the alternative PSTB area in SMAC 1 has been loaded. When set, causes system errors caused by SMAC Ø to use SMAC 1. If not set causes all system errors to use SMAC Ø.
	16 MULT	Set by software to indicate that this OCP is part of a multiprocessor. It also has the effect of making the photodump area dependant on the OCP port no.
	17 FSEI	Causes a software system error if set to 1.
	18 INHUB	Inhibit use bits.
	19 HOOT	The hooter emits a continuous 1 Kc note when this bit is set to 1.
	20 FSSNEQ	Inhibit stack slaving.
	21 LSSREJ	Lock stack slave rejection pointer.
	22 STCL	Stop clock and initiate DTU.
	23 IRETLOG	Inhibit retry logging interrupt.
	24 LISREJ	Lock instruction slave rejection pointe
	25 IACLOG	Inhibit ATU/Cache Logging Interrupt for successful retry.
	26	Unused.
	27 LOPREJ	Lock OP slave rejection pointer.
	28 INHOP	Inhibit OP slaving.
	29 DD (Double Dump)	Makes photodump area port dependent.

Note 1.

Those bits marked Unused or Hardware Use may be written to without causing a malfunction of the hardware.

Note 2.

These fields are bit significant with the lowest numbered bit corresponding to the lowest numbered module. If two Activates or two Interrupts occur at the same time priority is always given to the lowest numbered module.

6.3.2 cont Note 3.

4 Port SMAC

Module Number	Ø	1	2	3
Port Number	Ø	1	2	3
Geographical Processor Number (C = CPU, S = SAC)	S1	SØ	CØ	C1
PI Value in SSR	(-)	(-)	2	3

6.3.3 Inter-OCP Communication

To communicate with the other OCP, Load or Store ACC with image store format 42PØØØØM is used where P is the Port No. and M is the message as defined below.

M = Ø	Clear Slaves	
1	Remote IPL	IS Write
2	Remote register load	
3	Send Status	IS Read
4	Suspend	
5	Restart	
6	Clear MPI	IS Write
7	Illegal	

The contents of ACC (which must be single length) will be written to word 9 of the communication area, but will be ignored by the receiving OCP. Use of store B will be undefined.

Using an Image store write with message M = 3 or an Image store read with M = Ø, 1, 2, 4, 5, 6 or 7 is undefined, but will probably result in a lock up situation resulting in a System Error Timeout, or Post Timeout on subsequent use of the SMAC communication area.

Sending SAC image store (i.e. 44PØXXXX or 4ØPTXXXX) with an OCP port no. will result in a NACK from the receiving OCP, causing a Program Error in the sending OCP.

Using a message value M = 7 is undefined.

Setting P = Port No. of the sending OCP will cause a System Error Timeout.

6.3.3.1 Clear Slaves

This causes the slaves of the processor to be cleared in an orderly manner. The processor then continues processing. Acknowledge is sent to the initiating OCP after the slave stores have been cleared.

6.3.3.2 Remote IPL

This causes the processor to perform the pseudo-activate sequence which is normally started by the interrupt at the end of the IPL peripheral transfer. It is used in multiprocessors to bring the other OCPs into the system after the first OCP has been loaded.

Acknowledgement is sent to the other OCP before the IPL takes place.

6.3.3.3. Remote Register Load

This has the same effect as Remote IPL but the AU microprogram load is inhibited. Acknowledgement is sent to the other OCP before the register load takes place.

6.3.3.4 Suspend

This causes the processor to be suspended.

6.3.3.5 Restart

Used to restart the processor after a Suspend message, or after a System Error Interrupt.

6.3.3.6 Clear MPI

This causes the external multiprocessors interrupt bit MPIX to be cleared.

6.3.3.7 Send Status and Clear SEI

The status which corresponds to the parameter stacked on system error is read into A3, and the system error interrupt cleared.

This instruction is only meaningful if the interrogated OCP has signalled a system error and has suspended, and will always leave that OCP suspended.

Note that the system error parameter is also dumped on System Error.

6.3.3.8 Illegal Messages

An illegal combination of bits in bits 29 - 31 (i.e. 7) or bit 17 set, or SAC type image store to an OCP port (i.e. bit 6) will result in a NACK causing the sending OCP to program error, and will not interfere with the receiving OCP which will continue with normal instruction sequencing.

6.3.4 Multiprocessor Interrupt

Two bits in the configuration register can be set by software to cause a multiprocessor interrupt in either OCP.

S1 bit 22 - MPIS
causes an MPI to the sending OCP only.

S1 bit 23 - MPIX
causes an MPI to the other OCP only.

MPIX will normally be cleared by Inter processor image store "Clear MPI" from the other OCP.

MPIS will normally be cleared by image store write Ø to bit 22 of the configuration register. In order for an MPI to occur, Allow Normal Interrupts must be set in the receiving OCP i.e. for the case of MPIS the OCPs own port number must be set.

6.3.5. Broadcast System Error (SEIO)

If this bit is set, any incoming inter-OCP Image Store that normally allows the OCP to continue processing i.e. Clear Slaves, Restart, Clear MPI and Illegal Message will leave the OCP suspended. The SEIO must be cleared by "Send Status and clear SEI" before the OCP can be restarted. "Remote IPL" and "Remote Register Load" do not require this bit to be reset in order to work.

6.4. SMAC REGISTERS

6.4.1 4A20) SMAC CONFIGURATION REGISTER
6A20)

This register is written to in each SMAC by KRM-CONFIGURE-IN/OFF-OCP to unset/set bits 26 - 29. Bits 26 - 29 control whether that port is allowed to talk to that SMAC.

1 = closed to that port.

0 = open to that port.

6.5 SAC REGISTERS

6.5.1 4500) 6500) SAC LOWER WINDOW

This register is read by KRM-DUAL-OCP-TEST in each SAC known to the other OCP. It is read to ensure that the OCP being configured in can access the SAC(s) known to the first OCP. It it can't then the result code KRM-MPROG-LOAD-FAILS is returned.

7.1 To Configure an OCP In

(a) Ensure that the OCP is on 'run', and for 2960 that the TLOE cassette is in the ECP reader.

(b) On the SRU

If both OCPs are currently in the same configuration:-

1. Depress the appropriate change key.
2. Press enable and return. The OCP will now be 'free'.
3. Press enable and return. This will reset the OCP by sending a local IPL.
4. Reset the change key. The OCP will now be back in the configuration.

If the OCPs are in different configurations then to move OCP2 from configuration 'B' to configuration 'A':-

1. Depress the change key for OCP2 in configuration 'B'.
2. Press enable and return on configuration 'B'.
3. Reset change key. The OCP will now be free.
4. Depress the change key for OCP2 in configuration 'A'.
5. Press enable and return on configuration 'A'. This will reset OCP2 by sending a local IPL.
6. Reset the change key. OCP2 will now be in configuration 'A'.

(c) On 2960, wait until the status 'stopped' light goes out, indicating that IPLM has loaded off the cassette.

(d) CDS OCPn, IN.

4.11 HARDWARE SYSTEM ERROR PARAMETER - 2960

System Error

Hardware System Error	(32 bit word)
Bits 0 - 2	Failing Module No. If the system error is reported in a processor other than the originating module, i.e. if bits 0-2 of the parameter are not equal to the module number of the reporting processor, bits 3-31 of the parameter are zero.
Bits 3, 4	01 Irrecoverable Error 10 Successful Retry 11 Retry Failed (Code 00 used for Software System Error)
Bits 5 - 7	Zero
Bits 8 - 11	ACR
Bit 12	Zero
Bit 13	0 Photograph taken 1 No Photograph
Bit 14	0 SSN+1 OCP Register Dump 1 No SSN+1 Dump
Bit 15	0 Full Photograph)valid only 1 Mini only)if bit 13 = 0
Bits 16 - 31	Signify the failing Sub-Module (if bits 3, 4 ≠ 0, 0)
Bit 16	SMAC system error including Multibit Hamming failure
Bit 17	Single bit (recovered) Hamming failure.
Bit 18	Decoder Parity Error
Bit 19	SAU Parity Error
Bit 20	Store time out
Bit 21	OCP Internal time out
Bit 22	Microprogram Engine Parity
Bit 23	Data Parity Error from SMAC
Bit 24	Microprogram detected error

Bits 25 - 31

Other bits to be defined for internal OCP-detected failure Bits 16, 17 and 20 are used for the same purpose on 2970.

4.12 SOFTWARE SYSTEM ERROR PARAMETER - 2960

(32 bit word)

Bits 0 - 2	Module Detecting failure
Bits 3, 4	0, 0 Software System Error
Bits 5 - 7	Zero
Bits 8 - 11	ACR
Bits 12 - 15	Zero
Bit 16	Illegal Virtual Store condition
Bit 17	Class 5 Interrupt Masked (VSI)
Bit 18	Class 7 Interrupt Masked (PEI)
Bit 19	Class 8 Interrupt Masked (System Call)
Bit 20	Class 9 Interrupt Masked (Out)
Bit 21	Class 10 Interrupt Masked (Extra code)
Bit 22	Stack Segment Number is ODD
Bit 23	Segment Table Format Error
Bit 24	Entry Forced by Software (Image Store)
Bit 25	ACS = Ø on Initial Activate
Bits 26 - 31	-

N.B. 4014000F indicates a forced dump.

5.2 Layout of KEM-Store- Allocation

5.2.1 2960

Real Address (bytes)

HEX	DECIMAL	
4C-5F	76-95	Software System Error parameter
60-63	96-99	Hardware stacked SEI parameter
64	100	Type of unit (HM_OCP) = X'91'
65	101	PORT number
66-67	102-103	The length of the rest of the OCP part of the log
68-7F	104-127	Unused
80-BF	128-191	Copy of SSN+1 registers
C0-C7	192-199	LSTBØ, 1
C8-CF	200-207	PSTBØ, 1
D0-FF	208-255	Unused
100-1FF	104-511	The OCP Photograph for PORT 2
200-2FF	512-767	The OCP Photograph for PORT 3

The next section will be variable in length depending on the number of SMACs. For each SMAC in the system, the following 20 byte areas will be produced:-

Ø	Type of Unit (HM_SMAC) = X'92'
1	SMAC number
2-3	Size of rest of this entry (16)
4-7	Failing data for this SMAC (4COS6004)
8-11	Failing address for this SMAC (4COS6100)
12-15	Failing status for this SMAC (4COS6A00)
16-19	Configuration for this SMAC (4COS6A20)

6.1 cont

Bit 14 - 0 Cause MPI on completion of IS Command

= 1 Cause SEI on completion of IS Command

Bit 15 This bit defines where the MPI/SEI caused by Bit 14 is to be sent.

= 0 The interrupt is sent to the port other than the one specified in the IS Command and it is generated as if it is an External Interrupt, i.e. an IS location must be read to clear it.

= 1 The interrupt is sent to the port specified in the IS Command and it is generated as if it is an Internal Interrupt, i.e. entering the software interrupt procedure via the IST clears the interrupt.

N.B. Bits 14 and 15 determine the type and destination of interrupt to be generated after the IS access to the specified address has been completed.

6.2 CPU REGISTERS (2960/2970)

6.2.1 6009 BROADCAST SYSTEM ERROR

This register controls whether System Errors are to be broadcast to the other OCP or not.

Bit 31 = 1 Broadcast SE
= 0 Don't broadcast SE

In normal dual running Bit 31 is set in both OCPs so that when either OCP SE's it is broadcast to the other OCP. On receipt of a SE from the other OCP bit 31 of 6009 (in the OCP handling the system error) is cleared by hardware. Bit 31 can be reset by software after SEI-ANALYSER has decided whether it is going to carry on using the failing OCP.

Broadcast System Errors is turned on in the OCP being configured in by KRM-DUAL-OCP-TEST and in the other OCP by KRM-CONFIGURE-IN-OCP.

It is turned off either by hardware or KRM-CONFIGURE--OFF-OCP.

6.2.2 600A SYSTEM INTERRUPT MASK

This register controls communications between port connected devices.

Bits 24 - 27 = SA (ACTIVATES) = MBI bits 8-11 on 2960
28 - 31 = SI (INTERRUPTS) = MBI bits 12-15 on 2960

Bits 24 & 28 Control Port 0
25 & 29 Control Port 1 etc.

If a bit is set in SA then it inhibits activates being sent to that port.

If a bit is set in SI it inhibits interrupts from that port.

On a dual system the following applies: the IPL OCP can receive interrupts from and send activates to all ports, the non IPL OCP cannot receive interrupts from the SAC(s) on the system but can send activates to all ports. The reason the non-IPL OCP is closed to the SAC(s) is so that on peripheral interrupts both OCPs don't go for the PERM CPU SEMAPHORE resulting in one OCP servicing the interrupt and the other looping on the semaphore (when the looping OCP gets the semaphore it would fall through PERM-SERVICE-RESPONSE as the interrupt has been serviced).

The bit settings of SA/SI corresponding to the port number of this OCP are ignored.

i.e. for port 3 bits 27 & 31 are irrelevant
port 2 bits 26 & 30 are irrelevant

6.2.3 6012 LOAD MICROPROGRAM

This register controls loading the microprogram to the OCP being configured in. KRM-CONFIGURE-IN-OCP calls KRM-GIVE-MICROPROGRAM to get the OCP microprogram and place it in SMAC Ø BLOCK Ø. Whilst the OCP microprogram is in block Ø photographs are inhibited by writing to IS 6011.

6.2.4 6302 SYSTEM ERROR INTERRUPT

This register is read by SEI ANALYSER (in the OCP that had a SE) in order to clear down the SE.

When KRM-DUAL-OCP-TEST is running in the OCP being configured in it reads this register so that the OCP is not declared to the system with a system error pending.

6.2.5 6303 MULTIPROCESSOR INTERRUPT

This register is read by KRM-HANDLE-MPI or VMM-MULTI-OCP-INT-HANDLER to clear down MPI's generated on successful Configure-In or Process-Reschedule respectively.

6.2.6 2960 M.B.I. (w.s. = 16)

0	EVENT PEND
1	
2	
3	
4, 5	1900 DEC.SLOT.No.
6, 7	S4 DEC.SLOT No.
8-11	SI MASK INHIBIT PORTS 0-3 TX Activate
12-15	SI MASK INHIBIT PORTS 0-3 RX Interrupts
16	JUMP CONDITION TRUE
17	DO NOT USE μ-PROG SYS.CALL CODE.
20	IST ACCESS
21	APSTB (WD's 0,1 SMAC 1)
22	SSN+1 DUMP
23	BROADCAST SEI
24	MPI
25	SEI
26	EXIS
27	COMMUNICATION SMAC No.
28, 29	CLOCK MODULE No.

HELP

Should the HELP line be pulled by a bit being set in the HELP register (see 3.6.1) then the resulting action is shown in the flowchart, on the following page.

The flowchart refers to the options set in WS 27 whose contents can be set as follows:-

WS #27			Set by
BITS	0 - 14	Spare	
15	-	Error handling in progress	ECP during photo procedure
16 - 19	-	Reserved	
17	-	Stop after photo	*Type "HELP" on ECP
20	-	Stop on SEI	System Software or *Type "HELP OFF" on ECP
21	-	Stop on PEI	Syst. Soft/Operator
22	-	Photo on PEI	Syst. Soft/Operator
23	-	Reserved	
24	-	Inhibit Hamming Correction Reporting.	Syst. Soft/Micro prog.
25 - 27	-	Reserved	
28	-	Inhibit data slave	
29 - 30		Reserved	
30 —		ATS.	
31 = 1 ⧈		Inhibit full photo (for Soft or External SE-No Photo) (for P.E. and u-prog detected errors - Mini photo).	Syst. Soft.

ECP COMMANDS:-

* "HELP" - Takes immediate photograph and halts.

"HELP OFF" - HELP Reg. displayed and halts. (No photo).

"HELP ON" - Restores Normal handling.

HELP HANDLING Various parts of photo collected by ECP or MICOS