ELLIOTT

MCS 920B
FACTS

FACTS FOR ENGINEERS

The M.C.S. 920B is a rugged and compact digital computer that is particularly suited to the solution of on-line real time problems. Some typical applications are:

Mobile systems for Air Traffic Control, Combat Data Handling, etc.;
Navigation;
Weapon and fire control systems;
Control of satellite tracking aerials;
Industrial uses.

The Computer can be supplied in two packs, sealed case or 19 in. rack. Generally the former meets the British Military Defence Specification D.E.F. 133 (L3). Silicon semi-conductors are used throughout giving a working temperature range of −10°C to +55°C.

The arithmetic unit of the computer forms a loop comprising the five basic registers and adding unit, in which the computer carries out its addition, subtraction and shifting operations. Gating conditionals produced by the control module, in response to the micro-program, manipulate the program operands within the loop in accordance with the instruction. The program control unit regulates the allocation of computer time when it has to be shared between programs. It can interrupt one program in order to enter and take action in another of higher priority. Thereafter, the computer will select the next program with the highest priority that is waiting for attention. These features of priority interrupt and instruction modification give an effective increase in speed over other computers without these facilities.

PHYSICAL CHARACTERISTICS

	Depth	Width	Height	Weight
Computer	8¾ in.	18¼ in.	32 in.	90 lb.
Military pack	(21·3 cm.)	(47·3 cm.)	(81·2 cm.)	(40·8 Kg.) (8192 word store)
Computer				
Standard 19 in.	8¾ in.	19 in.	31½ in.	75 lb.
Rack Mounting	(22·6 cm.)	(48·3 cm.)	(80 cm.)	(34 Kg.) (8192 word store)
Power Unit	15¹³⁄₁₆ in.	17⁷⁄₁₆ in.	8¾ in.	35 lb.
Military pack	(40·6 cm.)	(44·3 cm.)	(22 cm.)	(15·8 Kg.)
Power Unit				
Standard 19 in.	13¹³⁄₁₆ in.	19 in.	8¾ in.	45 lb.
Rack Mounting	(35·5 cm.)	(48·3 cm.)	(22 cm.)	(20·4 Kg.)
Control Unit	6½ in.	20 in.	7¼ in.	16 lb.
Free Standing	(16·5 cm.)	(50·8 cm.)	(17·9 cm.)	(7·3 Kg.)
Control Unit				
Standard 19 in.	6 in.	19 in.	5¼ in.	8 lb.
Rack Mounting	(15·2 cm.)	(48·3 cm.)	(13·3 cm.)	(3·6 Kg.)

POWER SUPPLIES

D.C. Inputs: 20–30V D.C.
Single Phase Input A.C. (50–60 c.p.s. ±10%)
200–250V A.C. ±10% 100–125V A.C. ±10%
Three Phase Input A.C. (400 c.p.s. ±10%)
204V ±10% 117·5V ±10%

FACTS FOR PROGRAMMERS

The M.C.S. 920 model B is a parallel computer with an 18 bit word length and an internal memory of 8192 words. The store may be extended to a maximum of 65536 words by the external addition of store blocks of 8192 words or 16,384 words. If extra store units are fitted an autonomous data transfer facility may be utilised. This facility provides for the transfer of data between extra store units and peripheral equipments without going through the computer registers, thus allowing transfer to proceed concurrently with computation. The A.D.T. facility may also be used to enable two computers to share common extra store units. 8 hole paper tape is used of which the fifth digit (from the least significant end of the character) is a parity bit and is ignored on input. There are 16 basic functions governed by a built-in micro-program. The sign of the number is represented by the most significant digit with the binary point placed immediately after this bit. Positive numbers are represented directly and negative numbers by their complement with respect to two. The range of numbers that may be represented in the computer is thus from -1 to $+1\ -2^{-17}$.

When a word represents an instruction, its bits are grouped as follows:

B	F	N
Modifier	Function	Address

Bits 1 to 13 –'N'– Address bits which specify any one of 8192 store locations.
NOTE: When additional storage is used the J Register will hold a 16 bit address.

Bits 14 to 17 –'F'– Function bits which specify the operation to be carried out.

Bit 18 –'B'– The modifier bit which if it is a
0 . . . the instruction is obeyed as stored, and if it is a
1 . . . the address bits are modified, before the instruction is obeyed, by the addition of the contents of the B Register. The function bits remain unaltered, the version of the instruction held in store remaining unchanged.

The Control Unit provides either manual or automatic control over the computer. It can also be used to test operation of the computer independently of its peripheral system.
In the 'AUTO' mode, only power ON/OFF and RESET controls are operative. When switched ON in this mode, the computer jumps to the program trigger location 8177 and commences operation.
The number generator keys are operative for setting up starting addresses when the Mode Switch is either in the 'OPERATE' or 'TEST' position. The Control Unit provides the following: Power ON/OFF, Computer Stop, Computer Restart, Computer Reset, Jump. With the Mode Switch in the 'TEST' position the following special test controls can be operated: Order Stop/Cycle Stop, Cycle Repeat, Enter, Obey.
A loudspeaker with volume control is provided as an audible means of identifying individual program operation.
Priority level operation and indication is effected by three buttons and indicators, one for each level.

920 TELECODE

NOTE: Tapes using this telecode are read without parity check with mode switch on paper tape controller in position 1. Position 2 allows tapes using the A.S.C.I.I. format to be read. Position 3 allows all 8 tracks of the tape to be read.

Character	*Numerical Value*	*Elliott (920) Meaning*	*Character*	*Numerica Value*	*Elliott (920) Meaning*
Zone 0			***Zone 2***		
00000.000	0	Blank	01010.000	32	;
00010.001	1		01000.001	33	A
00010.010	2	NewLine(CRFL)	01000.010	34	B
00000.011	3	Throw Tab	01010.011	35	C
00010.100	4		01000.100	36	D
00000.101	5		01010.101	37	E
00000.110	6		01010.110	38	F
00010.111	7		01000.111	39	G
00011.000	8	(	01001.000	40	H
00001.001	9	)	01011.001	41	I
00001.010	10	,	01011.010	42	J
00011.011	11	£	01001.011	43	K
00001.100	12	:	01011.100	44	L
00011.101	13	&	01001.101	45	M
00011.110	14	*	01001.110	46	N
00001.111	15	/	01011.111	47	O
Zone 1			***Zone 3***		
00110.000	16	0	01100.000	48	P
00100.001	17	1	01110.001	49	Q
00100.010	18	2	01110.010	50	R
00110.011	19	3	01100.011	51	S
00100.100	20	4	01110.100	52	T
00110.101	21	5	01100.101	53	U
00110.110	22	6	01100.110	54	V
00100.111	23	7	01110.111	55	W
00101.000	24	8	01111.000	56	X
00111.001	25	9	01101.001	57	Y
00111.010	26	10	01101.010	58	Z
00101.011	27	11	01111.011	59	
00111.100	28	=	01101.100	60	
00101.101	29	+	01111.101	61	
00101.110	30	-	01111.110	62	Vert Bar
00111.111	31	.	01101.111	63	

920 TELECODE

Character	Numerical Value	Elliott (920) Meaning
Zone 4		
10010.000	64	Space
10000.001	65	
10000.010	66	
10010.011	67	
10000.100	68	
10010.101	69	
10010.110	70	
10000.111	71	
10001.000	72	
10011.001	73	
10011.010	74	
10001.011	75	
10011.100	76	stop code
10001.101	77	
10001.110	78	
10011.111	79	
Zone 5		
10100.000	80	
10110.001	81	
10110.010	82	
10100.011	83	
10110.100	84	
10100.101	85	
10100.110	86	
10110.111	87	
10111.000	88	[
10101.001	89	]
10101.010	90	10 (suffix)
10111.011	91	<
10101.100	92	>
10111.101	93	↑
10111.110	94	~
10101.111	95	%

Character	Numerical Value	Elliott (920) Meaning
Zone 6		
11000.000	96	?
11010.001	97	a
11010.010	98	b
11000.011	99	c
11010.100	100	d
11000.101	101	e
11000.110	102	f
11010.111	103	g
11011.000	104	h
11001.001	105	i
11001.010	106	j
11011.011	107	k
11001.100	108	l
11011.101	109	m
11011.110	110	n
11001.111	111	o
Zone 7		
11110.000	112	p
11100.001	113	q
11100.010	114	r
11110.011	115	s
11100.100	116	t
11110.101	117	u
11110.110	118	v
11100.111	119	w
11101.000	120	x
11111.001	121	y
11111.010	122	z
11101.011	123	
11111.100	124	
11101.101	125	
11101.110	126	horiz. bar
11111.111	127	Erase

INSTRUCTION EXECUTION TIMES

Quoted below are the nominal times in micro-seconds for the execution of each instruction including: (a) Accessing and incrementing the Sequence Control Register, 7; (b) Accessing the instruction, 9; (c) Executing the instruction (depends on instruction). They do not include: B Modification, 7.2 and this must be added where relevant.

The fixed overhead times for all instructions are:
16.5 μS for unmodified instructions
23 μS for modified instructions.

FUNCTION	TITLE	TOTAL EXECUTION TIME (UNMODIFIED) *8192 word store*
0	Set B Register	28.5 μS
1	Add	24 „
2	Negate and add	27 „
3	Store Auxiliary Register	23.5 „
4	Read	24 „
5	Write	23.5 „
6	Collate	23.5 „
7	Jump if Zero	26.5 „ Acc. Zero 21.5 „ Acc. +ve 20 „ Acc. −ve
8	Jump	24 „
9	Jump if Negative	26 „ Acc. −ve 20 „ Acc. +ve
10	Count in store	24 „
11	Store S.C.R.	31.6 „
12	Multiply	76.5 „
13	Divide	79.5 „
14	(a) Shift (b) Block Transfer	(a) 22+3n μS for Shift (b) 23.5+9.5n μS minimum for Block Transfer
15	(a) Input/Output (b) Program terminate	20.5 μS min. 20.5 μS

NOTE: n=number of places shifted or number of words in block. The Auxiliary Register acts as an extension to the accumulator, holding the least significant part of (a) the product (function 12), (b) the dividend (function 13), or (c) the operand (function 14). It should be noted that B modification affects its contents, as do instructions, 0, 2, 7, 9, 12 and 13. In particular, instructions 0 and 2 place the operand from the store in the Auxiliary Register. Thus the contents of the Auxiliary Register previously stored by instruction 3 can be reset in 60 micro-seconds by obeying instructions 0 or 2 followed by a left shift, whereas resetting by multiplication or shifting from the accumulator would take about 80 micro-seconds.

INPUT AND OUTPUT INSTRUCTIONS

If the most significant bit of N is zero, the instruction is an input instruction; otherwise it is an output instruction.
The instruction is further described by the N bits as follows:

15 N	(N≤2047)	18 bit number input to accumulator from the device specified by N.
15	2048	Input to the accumulator from the tape reader. The contents of the accumulator are shifted left seven or eight places (dependant on mode) and the character from the tape reader is placed in the seven or eight least significant bit positions.

15 N	(4096≤N≤6143)	18 bit number in the accumulator is output to device specified by N.
15	6144	Output from the accumulator via the paper tape punch. The eight least significant bits of the accumulator are output as an eight bit character on paper tape.
15	7168	"Program terminate" instruction.
14 N	(2048≤N≤4095)	Transfer n words of information from device specified by bits 1 to 11 of N into store locations m to m+n−1. m is the contents of the accumulator, n the contents of the auxiliary register.
14 N	(4096≤N≤6143	Transfer n words of information to device specified by bits 1 to 11 of N from store locations m to m+n−1.

PRIORITY LEVEL PROGRAM ORGANISATION

Each priority level has its own Sequence Control Register and B Register. These registers are locations in the store and can be referred to by program in the normal way.

PRIORITY LEVEL	B.REG. LOCATION	S.C.R. LOCATION
1	1	0
2	3	2
3	5	4
4	7	6

The Accumulator and the Auxiliary Register are shared between all four levels so they must be safeguarded by program every time an interrupt occurs. It will also usually be necessary to reset the Sequence Control Register on terminating a level so that the program, when next demanded, will start again at the same location. All these conditions are fulfilled by the following control instructions. They are applicable to any program on levels 1, 2 or 3 which starts at location N.

LOCATION	INSTRUCTION		REMARKS
	Function	*Address*	
[N−6]	—	—	Store for lower level AR.
[N−5]	—	—	Store for lower level Acc.
[N−4]	0	N−6	Reset lower level AR.
[N−3]	14	1	
[N−2]	4	N−5	Reset lower level Acc.
[N−1]	15	7168	Terminate, Note S.C.R. reset to N.
ENTRY[N]	5	N−5	Store lower level Acc.
[N+1]	3	N−6	Store lower level AR.
[N+]	—	—	Required program (x locations).
[N+2+x]	8	N−4	Jump to reset for lower level.

If the contents of the AR on the lower level are not required then instructions N−4, N−3 and N+1 can be omitted and store location N−6 is not required.

INITIAL INSTRUCTIONS

A set of permanently available Initial Instructions facilitates the reading of program tapes into the computer. These are obtained by entering the starting address 8181.
The initial instructions and their respective addresses for a 8192 word store are tabulated below.

ADDRESS	INSTRUCTION			EFFECT
'N' digits	'B'	'F'	'N'	
8180	/	15	8189	(−3)
8181		0	8180	(Set B-Register to −3)
8182		4	8189	(Set Accumulator initially)
8183		15	2048	(Shift and input tape character)
8184		9	8186	(Jump to 8186 if Accumulator is negative)
8185		8	8183	(Jump to 8183 if Accumulator is positive)
8186		15	2048	(Shift and input final tape character of word)
8187		5	8180	(Store word read in)
8188		10	0001	(Count in B-Register)
8189		4	0001	(Read B-Register)
8190		9	8182	(Jump to 8182 if Accumulator is negative)
8191		8	8177	(Jump to 8177 if Accumulator is positive)

Notes:

When entered at 8181 the routine initially reads words into 8177, 8178 and 8179, control is then transferred to location 8177. If these instructions set the B Register to −n and then transfer control to 8182, words can then be read into the sequence of n locations ending at 8179. Control is then transferred again to location 8177 so that a transfer instruction read into that location can trigger the program.
Rules for the punching of instructions and data in teleprinter code are given in the "920 Translation Input Routine". Further details can be found in the MCS 920 Program Library.

SYMBOLIC INPUT ROUTINE

S.I.R. enables programs to be written in modified machine code form. Essential details of S.I.R. are given below. Full details of S.I.R. can be obtained from the S.I.R. Handbook.

S.I.R. Symbols used for the Major Facilities

(i) IDENTIFIER	Group of up to six letters or numbers commencing with a letter.
(ii) CONSTANTS	
(*a*) Integer or fraction	±
(*b*) Octal groups	&
(*c*) Alphanumeric groups	£
(iii) ADDRESSES	
(*a*) Absolute	an unsigned integer
(*b*) Block relative address	N;
(*c*) S.C.R. relative	;±N

(*d*) Identified address	Identifier ± Integer (if required)
(*e*) Literal address	Any constant as in (ii) above or = followed by an instruction (absolute address only).
(iv) SKIPS	>+N
(v) COMMENT	( )
(vi) OPTION	*+N where N is the sum of the following.

1. Punch list labels.
2. Load and go operation (otherwise punch relocatable binary tape).
4. Clear the store up to the assembler.
8. Punch a binary loader tape
16. Continue assembly at location 8.
32. Set dictionary below the program.

(vii) Patches ↑+N
(viii) End of S.I.R. program %

When more than 1 tape is used only the last tape ends with % the others end with 'stop code' on a new line.

Note: Every new line symbol must be followed by at least four blanks.

START ADDRESSES

Initial assembly of S.I.R. tapes.

The S.I.R. assembly tape is read in under initial instructions. S.I.R. tapes are then read in at:

6017 (1011110000001) (START) for the first tape of a program.
6018 (1011110000010) (CONTINUE) for all other tapes.

The binary loader tape is read in by initial instructions. The RLB tapes can then be read in at:

7816 (1111010001000) (START A) for the first tape of a program.
7817 (1111010001001) (START B) for other tapes of the same program.
7818 (1111010001010) (START C) for the first tape of a new program when the previous program is to be left in the store.

ERROR INDICATIONS

Assembling

E0	F>15 or quasi-instruction wrong.
E1	Contextual error.
E2	Octal or alphanumerical error.
E3	Label used twice.
E4	Global identifier list error.
E5	Store full or patch error.
E6	Number overflow.
E7	Buffer overflow.
E8	Illegal character.
E9	Stop code not first on line.
EU	Unlocated identifier.

Loading

FA, FD	Misread or mispunched tape.
FC	Label used twice.
FE	Store full.
FF	Check sum failure.
FU	Unlocated identifier.

POWERS OF 2 IN DECIMAL

2^n	n	2^{-n}
2	1	.5
4	2	.25
8	3	.125
16	4	.062 5
32	5	.031 25
64	6	.015 625
128	7	.007 812 5
256	8	.003 906 25
512	9	.001 953 125
1 024	10	.000 976 562 5
2 048	11	.000 488 281 25
4 096	12	.000 244 140 625
8 192	13	.000 122 070 312 5
16 384	14	.000 061 035 156 25
32 768	15	.000 030 517 578 125
65 536	16	.000 015 258 789 062 5
131 072	17	.000 007 629 394 531 25
262 144	18	.000 003 814 697 265 625
524 288	19	.000 001 907 348 632 812 5
1 048 576	20	.000 000 953 674 316 406 25
2 097 152	21	.000 000 476 837 158 203 125
4 194 304	22	.000 000 238 418 579 101 562 5
8 388 608	23	.000 000 119 209 289 550 781 25
16 777 216	24	.000 000 059 604 644 775 390 625
33 554 432	25	.000 000 029 802 322 387 695 313
67 108 864	26	.000 000 014 901 161 193 847 656
134 217 728	27	.000 000 007 450 580 596 923 828
268 435 456	28	.000 000 003 725 290 298 461 914
536 870 912	29	.000 000 001 862 645 149 230 957
1 073 741 824	30	.000 000 000 931 322 574 615 479
2 147 483 648	31	.000 000 000 465 661 287 307 739
4 294 967 296	32	.000 000 000 232 830 643 653 870
8 589 934 592	33	.000 000 000 116 415 321 826 935
17 179 869 184	34	.000 000 000 058 207 660 913 467
34 359 738 368	35	.000 000 000 029 103 830 456 734
68 719 476 736	36	.000 000 000 014 551 915 228 367

SOME USEFUL CONSTANTS

$\pi = 3.141\ 592\ 653\ 590$

$\log_{10} e = 0.434\ 294\ 481\ 903$

$\log_{10} 2 = 0.301\ 029\ 995\ 664$

$\sqrt{2} = 1.414\ 213\ 562\ 373$

1 radian $= 57.295\ 779\ 513\ 082°$

$1/\pi = 0.318\ 309\ 886\ 184$

$\log_e 10 = 2.302\ 585\ 092\ 994$

$e = 2.718\ 281\ 828\ 459$

$\sqrt{3} = 1.732\ 050\ 807\ 569$

$1° = 0.017\ 453\ 292\ 520$ radian

TABLES OF BINARY

The purpose of these tables is to assist in the setting of binary addresses

1. Select the highest multiple of 64 less than (or equal to) the required
2. Set the first 7 switches (from the left) to the binary equivalent of the
3. Set the last 6 switches to the binary equivalent of the difference

TABLE A

Multiple of 64	*Binary Equivalent*	*Multiple of 64*	*Binary Equivalent*	*Multiple of 64*	*Binary Equivalent*
0	0000000	2048	0100000	4096	1000000
64	0000001	2112	0100001	4160	1000001
128	0000010	2176	0100010	4224	1000010
192	0000011	2240	0100011	4288	1000011
256	0000100	2304	0100100	4352	1000100
320	0000101	2368	0100101	4416	1000101
384	0000110	2432	0100110	4480	1000110
448	0000111	2496	0100111	4544	1000111
512	0001000	2560	0101000	4608	1001000
576	0001001	2624	0101001	4672	1001001
640	0001010	2688	0101010	4736	1001010
704	0001011	2752	0101011	4800	1001011
768	0001100	2816	0101100	4864	1001100
832	0001101	2880	0101101	4928	1001101
896	0001110	2944	0101110	4992	1001110
960	0001111	3008	0101111	5056	1001111
1024	0010000	3072	0110000	5120	1010000
1088	0010001	3136	0110001	5184	1010001
1152	0010010	3200	0110010	5248	1010010
1216	0010011	3264	0110011	5312	1010011
1280	0010100	3328	0110100	5376	1010100
1344	0010101	3392	0110101	5440	1010101
1408	0010110	3456	0110110	5504	1010110
1472	0010111	3520	0110111	5568	1010111
1536	0011000	3584	0111000	5632	1011000
1600	0011001	3648	0111001	5696	1011001
1664	0011010	3712	0111010	5760	1011010
1728	0011011	3776	0111011	5824	1011011
1792	0011100	3840	0111100	5888	1011100
1856	0011101	3904	0111101	5952	1011101
1920	0011110	3968	0111110	6016	1011110
1984	0011111	4032	0111111	6080	1011111

EQUIVALENTS

on the word generator.

address, and work out the difference (if any).
multiple, working from Table A.
working from Table B.

TABLE B

Multiple of 64	*Binary Equivalent*	*Difference*	*Binary Equivalent*	*Difference*	*Binary Equivalent*
6144	1100000	0	000000	32	100000
6208	1100001	1	000001	33	100001
6272	1100010	2	000010	34	100010
6336	1100011	3	000011	35	100011
6400	1100100	4	000100	36	100100
6464	1100101	5	000101	37	100101
6528	1100110	6	000110	38	100110
6592	1100111	7	000111	39	100111
6656	1101000	8	001000	40	101000
6720	1101001	9	001001	41	101001
6784	1101010	10	001010	42	101010
6848	1101011	11	001011	43	101011
6912	1101100	12	001100	44	101100
6976	1101101	13	001101	45	101101
7040	1101110	14	001110	46	101110
7104	1101111	15	001111	47	101111
7168	1110000	16	010000	48	110000
7232	1110001	17	010001	49	110001
7296	1110010	18	010010	50	110010
7360	1110011	19	010011	51	110011
7424	1110100	20	010100	52	110100
7488	1110101	21	010101	53	110101
7552	1110110	22	010110	54	110110
7616	1110111	23	010111	55	110111
7680	1111000	24	011000	56	111000
7744	1111001	25	011001	57	111001
7808	1111010	26	011010	58	111011
7872	1111011	27	011011	59	111011
7936	1111100	28	011100	60	111100
8000	1111101	29	011101	61	111101
8064	1111110	30	011110	62	111110
8128	1111111	31	011111	63	111111

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