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A BEAM-DEFLECTION VALVE FOR USE IN DIGITAL COMPUTING CIRCUITS

By M. W. ALLEN, B.E., Student.

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SUMMARY

Different methods used in the logical design of computing circuits are summarized, and from these, desirable properties are suggested for a universal computing element.

A description is given of a ribbon-beam-deflection valve based on these suggestions. Methods of application are illustrated with circuits and oscillograms using a single valve alternatively for binary addition, binary subtraction, or control of an output gate by various multivibrator circuits.

(1) INTRODUCTION

It has been appreciated for some time that the conventional grid valve is not ideal for switching circuits, since simple operations often require several valves. Consequently digital computers use large numbers of valves and components, which seriously affect their reliability. Various proposals have been made for universal switching elements in an attempt to reduce the total amount of equipment and the variety of circuits. A background to the idea of universal elements is provided by the various symbols and methods used in logical design. These will be briefly reviewed.

A system based on the analogy to the nervous system was developed by von Neumann[2] and others from the work of Pitts and McCulloch, who proposed a description of the nervous system based upon "two indication elements." These elements, which they called neurons, have the following properties: each neuron has an output line and a number of input lines. The input lines carry stimuli to excite or inhibit a signal on the output line (the response being immediate). All the signals are bi-valued, i.e. of the on-off type and not continuous. An "all or none" output response changes when the number of simultaneous inputs exceeds a certain number, called the threshold of the neuron. Some of the symbols used and their characteristics are shown in Fig. 1. The number in the circle is the threshold of the neuron; an inhibit stimulus overrides all excitation stimuli.

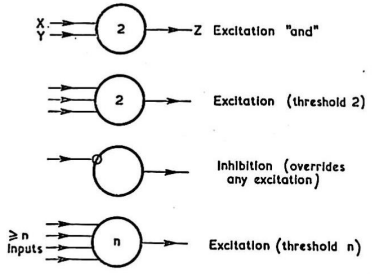

Fig. 1.—Neuron symbols.

Different connections of these elements can be written, using the rules of Boolean algebra. A difficulty arises in practice from the fact that there is very little correspondence between these symbols and the appropriate vacuum-tube circuits. Several modified schemes have been proposed to overcome this difficulty.

One method[4] uses special symbols rather than neurons to represent the valve circuits, and associated with each symbol is an algebraic operator; also included are Tables which list the different switching combinations of up to four variables in terms of these operators. (The switching combinations represent all the possible arrangements for four bi-valued inputs and a single bi-valued output). The operator expressions can be converted to symbolic form from which detailed circuits can be drawn. These Tables show that considerably more vacuum tubes are required than neurons for a given switching function. A number of other similar schemes have also been developed.

There appear to be two alternative solutions to simplify circuits. The first is to use only a single basic element, different combinations of this being used to derive the other elements. Several devices have been proposed on this basis. Speedy[3] has described a special valve and circuit which combines the properties of a trigger circuit and two electronic gates, and has illustrated how this may be used as a building block.

Another proposal[1] is the universal decision elements shown in Fig. 2. The switching Table is written as a form of matrix.

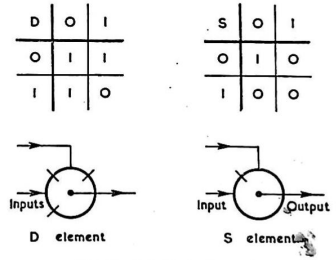

Fig. 2.—Decision elements.

The two input signals, each having possible values of 0 or 1, form the upper and left-hand side, and the output from the element, which can likewise be 0 or 1, is given by the intersection. In the symbol which is used to represent this matrix, a short line through the circumference indicates that the output is a 1 in the corresponding quadrant of the matrix. The universal elements are the D and S elements. One reason for the choice of these simple elements with two inputs and one output is that they are easier to analyse. More complex elements having more than two inputs and more than one output, although unwieldly in logical systems, may be useful in practice.

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Mr. Allen is in the Mathematical Instruments Section, C.S.I.R.O., Australia.

The following are suggested as desirable properties in a device to be used in a somewhat similar way to neurons:

(*a*) Four inputs, two of each polarity, to be used as excitation and inhibit connections. These inputs should preferably be of equal sensitivity, and such that direct links can be made between elements.
(*b*) Output terminals to give positive or negative signals.
(*c*) Complete isolation between inputs, and between inputs and outputs, so that they do not interact with each other.
(*d*) A power gain sufficient to drive as many as three other elements in paral el.

The present paper describes a ribbon-beam-deflection valve consisting of two interconnected elements, each having the above properties. The reason for this particular choice is that it enables binary addition, subtraction and other operations of interest to be carried out in a single valve which is limited to a 12-pin base. The application of the valve is illustrated with circuits and oscillograms.

It is interesting to observe that a still more useful element would be one whose proportions were capable of simple dynamic control. An example of such an element would be one which could be changed from addition to subtraction on application of a control signal derived from the previous operation, or from an external source. Similar elements are useful in logical systems, and would be equally useful in automatic computing. At present they seem difficult to realize practically.

(2) DESCRIPTION OF VALVE

Fig. 3 shows the essential features of one of the valves used. The valve is approximately 2¼in long and 1¼in in diameter. It

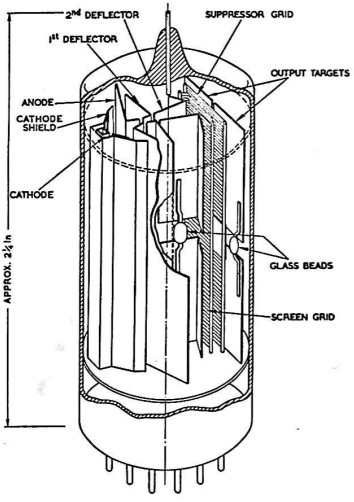

Fig. 3.—Valve details.

consists of a simple electron gun producing a ribbon-type beam which is directed axially outwards but deflected by sets of deflectors through screen and suppressor grids on to collecting targets. The direct voltage of the deflectors is half that of the anode producing a focusing field and assisting the repulsion of secondary electrons from the anode. The second deflectors are divided so that they can act independently on their respective sections of the beam. The beam is divided into sections before reaching the targets by a strip across the suppressor grid. Recent investigations have shown that considerable improvements would result from a back-to-back arrangement of sections using two sides of a common cathode. This would be the preferred arrangement for future work.

The essential elements of each section for design purposes are the arrangements of targets and deflectors. Each section has a divided target and two pairs of deflectors (the first pair of deflectors being common to both sections). The bottom pair of targets is divided centrally, and for the top pair the division is offset, so that with all the deflectors at the same potential, the beam divides centrally between the targets in the bottom section, and lies wholly on one target in the top section. The sensitivity of all the deflectors is the same, and their d.c. level is the same as that of the targets, so that direct links can be made between targets and deflectors. These properties simplify circuit arrangements.

The input signals applied to the deflectors are normally negative voltage pulses. The output signal is then taken as a corresponding negative voltage pulse from a load resistor attached to the target on which the beam impinges. In some cases positive voltage pulses are used, and these cases are distinguished by a primed letter. A corresponding positive output pulse occurs in a load resistor attached to the target from which the beam shifts on application of the input. A unit input pulse is considered as one which when applied to a deflector will shift the beam at the target a distance somewhat greater than one beam width.

Using the notation of Fig. 4 for the various deflectors and targets, it may be seen that the following equations relate the output target currents to the deflector-voltage inputs.

For the bottom section of the valve

$$i_{B1} = i, \text{ and } i_{B2} = 0$$

when $$D_2 - D_1 + D_{4B} - D_{3B} \geqslant \tfrac{1}{2} \quad . \quad . \quad . \quad . \quad (1)$$

and for the top section $i_{T1} = i$, and $i_{T2} = 0$

when $$D_2 - D_1 + D_{4T} - D_{3T} \geqslant 1 \quad . \quad . \quad . \quad . \quad (2)$$

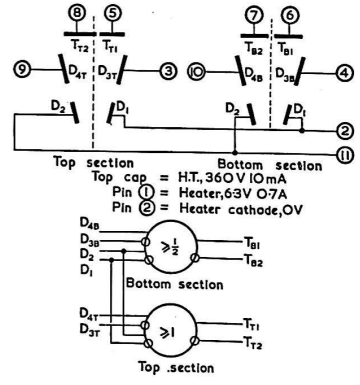

Fig. 4.—Base connections and symbol.

The relations may be summarized in the symbols of Fig. 4. Connections to deflectors which produce deflection of the beam in one direction are shown plain, while connections to deflectors which produce deflection in the opposite direction are indicated by a small circle surrounding the connection. Plain and circled connections to the targets are used to distinguish those parts on to which the electron beam is directed by negative pulses applied to similarly marked deflectors.

The numbers in the circle correspond to those in eqns. (1) and (2) and specify the conditions for current in the targets. This number is determined by the target offset, but it may be altered by a constant voltage difference on any deflector pair; thus by applying an appropriate bias to D_{3B} the number $\geqslant 1$ may be altered to $\geqslant 0$, $\geqslant 1$, $\geqslant 2$, etc.

(3) CIRCUIT APPLICATIONS

(3.1) Binary Addition

In forming the sum of two numbers, each step consists of the addition of the addend and augend, together with the carry digit from the previous step.

If n = Base of the number system.
x and y = Addend and augend digits.
C_{in} = Carry digit from the previous step.
S = Sum-digit output.
C_{out} = Carry-digit output.

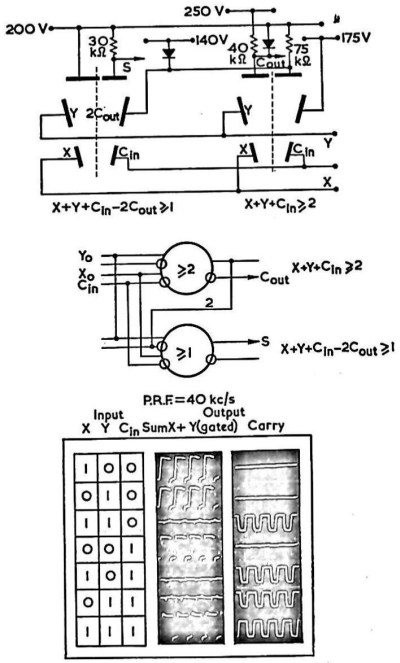

Fig. 5.—Binary addition.

then the rules for the output sum and carry digits may be stated as follows:

C_{out} occurs when

$$x + y + C_{in} \geqslant n \quad . \quad . \quad . \quad . \quad . \quad (3)$$

and S occurs when

$$x + y + C_{in} - nC_{out} \geqslant 1 = S \quad . \quad . \quad . \quad (4)$$

In the binary system, $n = 2$, and we have

$$C_{out} = 1, \text{ when } x + y + C_{in} \geqslant 2$$

and

$$s = 1, \text{ when } x + y + C_{in} - 2C_{out} = 1$$

These relations are similar to those given earlier relating target currents and deflector voltages. Fig. 5 shows these relations in symbolic form, and also the detailed circuit. The $\geqslant 2$ relation for the carry digit is obtained by a lower d.c. level on D_{3B}. In the circuit shown

x and y are supplied as negative voltage pulses of unit amplitude.
C'_{in} is a positive voltage pulse of unit amplitude.
$2C_{out}$ is obtained by using a load resistance sufficient to produce a voltage pulse of at least 2 units, clipped by a diode to reduce it accurately to 2 units.
C_{out} is a positive voltage pulse output.

It is apparent that spurious results can occur during the rise and fall of the various inputs. This does not necessarily cause complications in practice, since the results are always read into a storage register whose input gates may be closed during the transient period. In obtaining the waveforms shown the sum digits have been gated in this way. No spurious results can occur with the carry digits.

In the case of parallel addition, it is necessary only to connect the C'_{out} digit of one stage to the C'_{in} of the next.

Fig. 6 shows a two-digit parallel adder, and the waveforms illustrate some of the more interesting combinations involving a carry between stages.

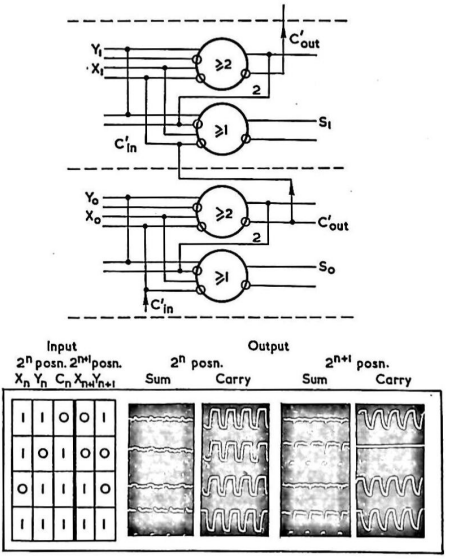

Fig. 6.—Parallel binary addition.

For a complete serial adder the C'_{out} digits must be delayed one digit period to provide the C_{in} digit for the following step. Fig. 7 shows a circuit which was operated at 120 kc/s with 5 microsec pulses. An amplifying valve is included in the $2C_{out}$ link to reduce transients, and a second valve feeds an 8-microsec delay line for the carry digits which are shaped by diodes to provide C'_{in}.

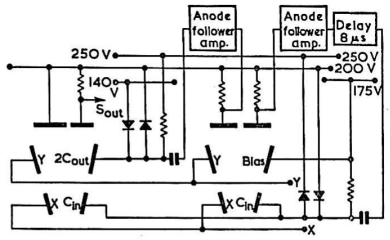

Fig. 7.—Serial binary addition.

(3.2) Binary Subtraction

Each step in the subtraction of the two numbers consists of subtraction from the minuend of the digits of the subtrahend, together with the borrow from the previous step, proceeding always from the least significant digit. The rules for binary arithmetic are as follows:

$$\text{Borrow } B_{out} = 1 \text{ when}$$
$$x - y - B_{in} \leqslant 1 \quad . \quad . \quad . \quad . \quad . \quad (5)$$
$$\text{Difference } D = 1 \text{ when}$$
$$x - y - B_{in} + 2B_{out} = 1 \quad . \quad . \quad . \quad . \quad (6)$$

Fig. 8 shows the symbolic form and the detailed circuit. The $\leqslant -1$ relation is achieved by a bias on D_{4B}.

x, y, and B_{in} are supplied as negative voltage pulses of unit amplitude.
$2B_{out}$ is obtained using resistances and a clipping diode.
B_{out} is taken from a dividing resistance.

As before, transient errors can occur during the rise and fall of the pulses, and these have been gated out.

Parallel and serial subtraction circuits can be made in a similar way to the corresponding addition circuits.

It is apparent that this method of circuit design may be applied to other switching circuits. The procedure is to examine the switching Table for relations between the input and output, of the following type:

$$D_1 - D_2 + D_{3B} - D_{4B} \geqslant \text{or} \leqslant n,$$
$$D_1 - D_2 + D_{3T} - D_{4T} \geqslant \text{or} \leqslant n_2$$

The requirements for binary addition and subtraction have resulted in the following design limits for the valve:

$$3 \geqslant n \geqslant -3$$
$$2 \geqslant D_1 - D_2 \geqslant -2$$

The relations should be checked to see that these limits are not exceeded.

The circuits which follow involve the control of a gate by a second element, and use the same valve as for binary addition and subtraction. They have been selected as the ones of most interest in digital computing.

(3.3) Bistable Storage

The application of the binary gating valve as a building block for switching circuits has been described by Speedy.[3] The two-section valve may be used similarly, except that only one gate is available. The circuit for a bistable section and coupled gate

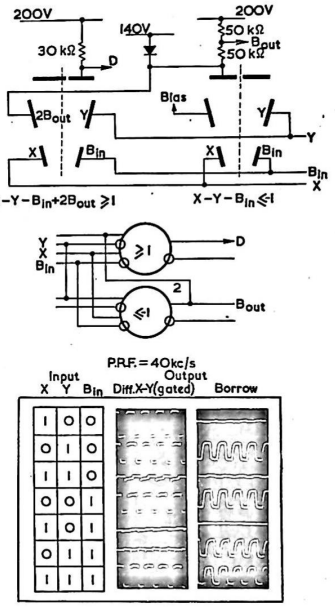

Fig. 8.—Binary subtraction.

is shown in Fig. 9. The symmetrically located targets are cross-connected to the common pair of deflectors, and to the supply voltage through load resistors. This results in two stable states, which may be switched by pulses on the second pair of deflectors.

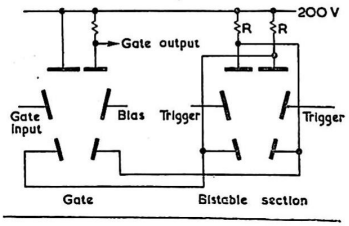

Fig. 9.—Bistable storage with an output gate.

The remaining section is then used as a gate coupled by the common pair of deflectors. The gate target is offset mechanically, and a bias is applied to D_{3B}, so that in one state the edge of the beam lies just off the target, and in the other it lies between one and two beam widths from the target. A unit pulse to the gate shifts the beam towards the gate target, so that the beam can strike the output target in one state and not in the other.

Fig. 10 shows a modification of this circuit to provide an input as well as an output gate. This circuit would be of use in static registers in a parallel machine.

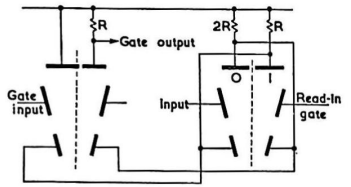

Fig. 10.—Register storage.

The load resistances for the symmetrical targets have been chosen as $2R$ and R, so that the second stable position is shifted one beam width further off centre. The state can only be switched by the coincidence of a digit pulse on D_{4B} and a positive gate pulse on D_{3B}. The read-out gate operates as before.

(3.4) Binary Counter

The action of the deflectors in a beam valve is in many respects equivalent to that of a grid in a triode. Thus circuits may be derived directly from equivalent grid-valve circuits. This has been done in the circuit shown in Fig. 11.

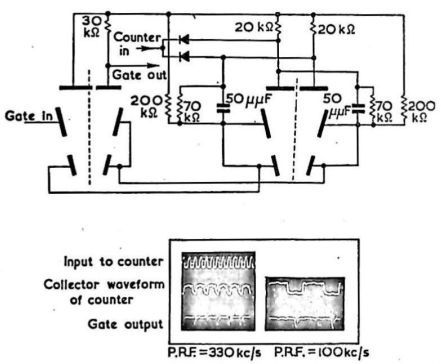

Fig. 11.—Binary counter with gate.

The direct link between target and deflectors is replaced by a resistance-capacitance network, and negative input pulses fed through diodes. The load resistances and the resistances of the cross-over network are chosen so that there are two stable states for the beam. A sharp negative pulse applied to the input diode causes the target at the high potential (no beam current) to follow the input, but transmits nothing to the other low-potential target. Because of the cross-coupling capacitor, the fraction of this which appears at the deflectors exceeds the steady-state value required for bistable action (which is determined by the resistances alone), and is sufficient to change the state. The following pulse switches the beam back, and so on.

In grid-tube circuits the switching speed is reduced by the loss in the step-down networks necessary because of the difference in d.c. level between the grids and anodes. In the beam valve the d.c. levels are the same, and the network loss can be minimized. This is the reason why beam valves with a much lower equivalent mutual conductance (in terms of milliamperes per volt on deflector or grid) perform comparably in such circuits. The waveforms of Fig. 11 illustrate the operation of the counter and coupled gate. Input pulses of about 2 microsec in width are applied to the counter, and identical pulses occurring midway between them are applied to the gate. Operation is shown at 100 kc/s and 330 kc/s, the latter being the limiting frequency.

(3.5) Multivibrators

It is apparent that, with the diodes separated, the circuit of Fig. 11 acts as a bistable multivibrator.

The bistable multivibrator can be converted to a monostable or astable multivibrator in exactly the same way as in grid-valve circuits. A monostable multivibrator is obtained by eliminating one resistor coupling a target to a deflector, but leaving in the capacitor. The beam can then remain in one stable state as before, but can only remain in the other state for a time dependent on the time for the discharge of the cross-coupling capacitor. One of the diodes can be omitted. Similarly, by eliminating both cross-coupling resistors, the circuit becomes equivalent to a free-running or a stable multivibrator. The remaining section of the valve can then be used as a coupled gate.

(4) ACKNOWLEDGMENTS

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