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# METROPOLITAN-VICKERS ELECTRICAL CO. LTD.,

(Member of the A. E. I. Group of Companies.)

TRAFFORD PARK, MANCHESTER, 17.

# ENGINEERING REPORT.

THE TYPE 950 GENERAL PURPOSE DIGITAL COMPUTER

FUNCTIONAL DESIGN.



**REPORT No.** 1026 Part 1.

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METROPOLITAN-VICKERS ELECTRICAL COMPANY LIMITED

ELECTRONICS DEPARTMENT
(RADAR DIVISION)

# ENGINEERING REPORT

No. 1026

## THE TYPE 950 GENERAL PURPOSE DIGITAL COMPUTER
## FUNCTION DESIGN

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Date December, 1955.

Approved L. W. BROWN.

Summary

The history of the design of the Type 950 Computer is traced back to a machine using Dekatrons. The way in which the machine is applied to the solution of a mathematical problem is explained and the basic units of the machine listed.

These are then considered in more detail. The use of a magnetic drum for all storage requirement is described and the way in which an instruction is obeyed is explained. Input and Output facilities and the controls and monitoring facilities available to the operator are described.

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# C O N T E N T S



## A P P E N D I C E S



## I L L U S T R A T I O N S

ILLUSTRATIONS (Continued)

# THE TYPE 950 GENERAL PURPOSE DIGITAL COMPUTER

## 1. INTRODUCTION

### 1.1 History

In the middle of 1954 investigations were started into the design of a general purpose digital computer utilizing the Dekatron cold cathode tube as a computing and storage element. Experience had shown that this tube was very reliable and it was considered that this reliability, together with its low power consumption and the fact that the whole computer would work in the decimal system, would make it a very suitable device on which to base the design.

By November 1954, investigations had shown that a computer based on the Dekatron was a practical proposition, and in fact some constructional work had already been done. At the same time the disadvantages of a decimal computer using the Dekatron compared to a binary machine were becoming obvious. Although the Dekatron worked in the decimal scale, other essential parts of the machine, such as magnetic storage, were essentially binary systems. Also the advantages regarding reliability and low power consumption were reduced by the fact that many thermionic valves would still be required. These facts, together with the knowledge that binary techniques would have much wider application, indicated that it would be more advisable to build a binary computer.

Once this was decided the possibility of using transistors to replace valves arose. Their use leads to great economies in space and power and although at the time the switching speed of the transistor circuits limited the speed of the computer, experience had been gained in their use and it is now evident that junction transistors capable of much higher switching speeds will shortly become available.

The first application of the computer was to be to the work of the Computing Section in M-V. Research Department which work is now being done on the Manchester University machine. The aim was to build a computer which would do this type of work and yet be appreciably cheaper than any other comparable machine.

After discussions with Research Department and some of the staff of the Computing Department at Manchester University a specification was arrived at (see Appendix 1). An instruction code was suggested by Research Department. This has been modified slightly after further discussions with them, and the present code is given in Appendix 2.

1.2 How the Computer is Used to Solve a Mathematical Problem

The machine is basically a device which will do arithmetic at a high speed under the control of instructions given to it by the operator. If advantage is to be taken of this high speed it must not be necessary to instruct the

machine every time it performs an operation as the time taken to do this would be far greater than the time the machine took to obey the instruction.

The characteristic is achieved by giving the machine a store which stores the data used in the calculations, and also the "programme" or list of instructions necessary to do the calculations. The speed of the machine depends to a great extent on how quickly it can read out of this store the data and instructions it needs, as it proceeds. Furthermore, the programme is written in such a way that repetitive mathematical processes are used as steps in the calculations. The computer may obey a small group of instructions many hundreds or thousands of times to obtain an answer and thus the time taken to instruct the computer to do this becomes comparable with the time taken by the machine to do the calculation. The computer must be able to decide when it has been round one group of instructions enough times, and when to progress on the next instructions. This is done as follows. Each instruction has included in it the "address" in the store of the next instructions to be obeyed, in addition to the instructions dealing with arithmetic operations. There are two addresses and they cause the computer to go one way or the other for its next instruction, depending on whether the sign of a certain number is positive or negative. Each repeated group of instructions contains one of these instructions and it is arranged that, when the group has been obeyed a sufficient number of times, the number being examined by this instruction changes sign and causes the machine to go to a new instruction outside the group.

In theory therefore the computer can solve any problem which is capable of being solved by simple arithmetic, however tedious they may be. Actually the solution of some problems is well suited to digital computer techniques whilst others are not.

## 2. REPRESENTATION OF NUMBERS AND INSTRUCTIONS

Numbers are converted to the binary notation before being put into the store. In the binary notation each digit represents a power of two instead of ten as in the decimal system.

Thus in decimals $321 = [3 \times 10^2] + [2 \times 10^1] + [1 \times 10^0]$

In binary $1010 = [1 \times 2^3] + [0 \times 2^2] + [1 \times 2^1] + [0 \times 2^0]$

It can be seen that each binary digit has only two values, "0" and "1" and therefore it is a very convenient system to use, since a digit may be represented by any device which has two states. In general this leads to a much simpler machine than one needing devices with ten states as required for the decimal system.

Numbers being fed from one part of the machine to another are represented by a series of pulses in time, the least significant digit being the first of the train, and the binary point occurring immediately before the most significant digit.

Negative numbers are represented by their complements modulo 2. Thus -N is stored as 2-N. If we restrict the numbers in the machine to $1 > N \geqslant -1$ it can be seen that the most

significant digit, known as the sign digit, will be 0 for positive numbers and 1 for negative numbers.

Numbers and instructions are both represented by a train of 36 digits known as a word. Only 32 digits are actually used to carry information, the first 4 being termed engineering digits and being used to provide time for the control system to operate in between words.

The word is divided into three syllables, S0, S1, and S2, each syllable being divided into twelve digit periods defined by P0 to P11. Thus any digit in a word may be defined by an S and a P pulse.

An instruction is constructed as shown in Figure 1. The digits P4 to P8 in S0 indicate what operation, out of the 26 available, is required and P0 to P11 in S1 give the address in the store to which that operation refers. Digits P0 to P11 in S2 indicate the address of the next instruction to be obeyed. The use of digits P9 to P11 in S0, the "B" digits, will be explained later under the heading "Control System".

## 3. THE BASIC UNITS OF THE COMPUTER

A simplified block diagram of the machine is shown in Figure 2. Lines connecting the various blocks indicate the paths that numbers and instructions may take during the operation of the machine. The gates which control these paths have not been shown in order to simplify the diagram.

The basic units are the main store and its associated address selection system, a smaller store called the B store an arithmetic unit producing the sum or difference of two numbers, the accumulator register, the instruction register, the multiplican register, and the E register, which all store information required during the calculation, a multiplier, an input device which enables information to be fed into the machine, an output device for recording the results, and a control system which organises the working of the machine.

3.1 The Main Store

The main store has a capacity of 4096 words which are held on a magnetic drum. The drum is approximately 5 inches high and 5 inches in diameter and runs at almost 3000 r.p.m. being driven by an induction motor. Its periphery is sprayed with a layer of magnetic oxide held in a cellulose base, about 0.001" thick. The drum eccentricity is about 0.002" and reading and writing heads are placed about 0.001" from the drum surface. A head consists of a single lamination of 0.015" thick mumetal with a 0.001" gap cut in it. Flux is induced in it by a 6 turn winding. The information is written on 128 separate tracks each with its own read-write head, and each track stores 32 words. Thus the digit frequency or "clock" frequency can be calculated from these figures.

Number of digits per revolution = 36 x 32.

Number of revolutions per sec. = 50.

Therefore clock frequency = 32 x 36 x 50 = 57.5 kc/s.

The phase modulation method of recording digits is used and waveforms are shown in Figure 3. A "one" is recorded by magnetising the drum coating in one direction during the first part of the digit period, and in the other direction the second part of the digit period. To record a "0" the directions of magnetisation are reversed.

Figure 3(a) shows the clock waveform and (b) shows a typical number. The flux distribution required is shown (c) and is produced by generating a voltage waveform of the form as shown in (c), converting this to a current waveform about zero, and passing this current through to the recording head. Information may be read from the drum by amplifying the voltage which is induced in the head. This has the form of Figure 3(d) and if it is amplified and strobed by the waveform shown in Figure 3(e) the original information can be recovered by suitable retiming and shaping. It will be noticed that the retimed waveform Figure 3(f) is necessarily one digit late, but this is allowed for in the design of the machine.

The selection of a particular address on the drum necessitates selecting the track required and generating a gate during the time the address required is passing under the head. A group of 7 staticizors, the coded track staticizors, are set by the 7 most significant digits of the address in the instruction, to the binary code of the track required. These staticizors provide the input for a diode matrix which selects the actual writing valve on the track required and also switches, by means of a diode switch, the output of that track into the

read amplifier. It is now necessary to gate the writing valve, or the read amplifier, whichever is required, during the time that the address called for is passing under the head. This is done by recording on a special track on the drum, called the address track, the address, as a binary number of each of the 32 words around the track. This is compared with the 5 least significant digits of the address required and a gate is generated when they agree.

The drum also has three special tracks which generate waveforms to control the timing of the computer. One generates the clock waveform which defines the digit period, another generates pulses which define the syllables in each word, and the third defines the words themselves.

3.2 The B Store

This holds 8 words only and takes the form of a regenerative track on the magnetic drum. A regenerative track consists of 2 heads working on the same track and spaced apart so that the track length between them will hold the required number of words, in this case 8. A diagramatic representation of this is shown in Figure 4.

Information is written onto the drum at W, and is read off again at R. The pulses are retimed to the clock waveform in the read amplifier and fed back to the write unit so that the information is kept recirculating around the loop. New information may be written in by allowing it to go to the write unit via gate G1 while the regenerative loop is inhibited by the gate G2. The contents of any address in the store may be read out by opening the gate G3 at the appropriate time.

## 3.3 The Arithmetic Unit & Accumulator

The arithmetic unit forms the sum or difference of 2 numbers which are fed to it. This unit uses the logical method of addition and subtraction and to understand this it is necessary to first consider what is meant by the 3 logical operations used.

The operation "and" on two binary digits gives a 1 in the result only if both digits were 1, otherwise it gives a 0.

The operation "or" on two binary digits gives a 1 in the result if either digit is 1.

The operation not equal ($\neq$) on two binary digits gives a 1 in the result only if the digits are different.

Since the numbers we are dealing with occur as a series of pulses in time, we form the sum or difference of each pair of digits in turn and therefore we must deal with the least significant first as this may produced a carry digit which may affect the more significant digits in the answer. Thus in general the arithmetic unit must produce the sum or difference of three digits, x, y, and $w_d$; $w_d$ being the carry digit from the previous digit, delayed by one digit period. The answer produced consists of 2 digits, $x \pm y$, and w, w being the carry digit to the next most significant place. Since the logical operations are performed on 2 digits only, the arithmetic operation must be carried out in two stages.

A table is given in Figure 5 showing how the 8 possible input combinations are operated on to give the required results for addition and subtraction. A block diagram is also given

showing the arrangement of logical circuits in the unit. It can be seen that the first part of the unit compares x and $w_d$ and produces output ($x \not\equiv w_d$) and (x "and" $w_d$). Then this output ($x \not\equiv w_d$) is compared with y to give $(x \not\equiv w_d) \not\equiv y$ and again with y if addition is required or with $(x \not\equiv w_d) \not\equiv y$ if subtraction is required to give $(x \not\equiv w_d)$ & y or $\{[(x \not\equiv w_d) \not\equiv y] \& (x \not\equiv w_d)\}$

It can be seen that the output of the second "not equals" circuit gives $x \pm y$ and the carry output w is formed by the outputs of the two "and" circuits being combined by an "or" circuit. In the machine the switch shown in Figure 5 to convert the unit from an adder to a subtractor is electronic and change over is controlled by a 2 state circuit set as required.

A diagram of the accumulator is shown in Figure 6. The actual storage is on a regenerative loop on the drum as for the B store, but in this case two words only separate the heads. Two words are necessary for the accumulator register since it is used to accumulate the product of the multiplication of two 32 digit numbers, which is a 64 digit number.

Numbers are added to, or subtracted from the accumulator by feeding them into one input of the arithmetic unit while the number already in the accumulator is fed into the other, the answer going back into the accumulator. During this operation, the regenerative loop between the output and input of the accumulator is inhibited.

A facility is available of multipling or dividing the contents of the accumulator by powers of 2 by the use of instructions which cause the stored number to be shifted in time. Referring to Figure 6, the normal regenerative loop of the accumulator is via the 1 digit delay D1 and the gate G2. Thus the actual delay due to the drum is arranged to be 1 digit less than 2 words. If a multiplication by $2^N$ is required, G2 is inhibited and regeneration allowed to take play via D1, D2, and G3, for N cycles. The contenets of the accumulator will then have been delayed by N digits, which is equivalent to multiplication by $2^N$.

If division is required, G2 is inhibited as before and regeneration takes place via G1 causing the digits to occur earlier.

It will be realised that the results of a arithmetic operation could give an answer which was outside the range of the machines 1 N -1. This must be guarded against by the programmer since, if it occurs, the accumulator will "overflow", because it cannot store the correct answer, and an error will result. If overflow should occur due to an error in the programme, a warning is given by a lamp on the control desk being lit.

3.4 The Multiplier

Multiplication in the binary scale is merely a series of shifts and additions, and is carried out in the following way. A separate instruction transfers the multiplicand from the store to the multiplicand, or D, register, where it is stored. This

register is a two word regenerative track similar to the accumulator. The multiply instruction transfers the multiplier from the store to the E register, a 1 word regenerative track, where the least significant digit is examined. If it is a 1 the contents of the multiplican register are added to the accumulator, otherwise no action is taken. The E register and the multiplicand register are now shifted so that the next most significant digit of the E register is examined and if it is a 1, the contents of the multiplicand register, which have now effectively been multiplied by 2, are added to the accumulator. This process is repeated until all the 1's in the E register have been sampled. This system works for both positive and negative numbers except for 1 modification when the multiplier is negative. In this case when the most significant digit of the E register is reached, which will be a 1 since it is a negative number, the contents of the multiplicand register are subtracted from, not added to, the accumulator. The mathematical proof of this will be found in Appendix 3.

3.5 The Control System - How an Instruction is Obeyed

The control system may be broadly divided into two parts, the sequencing unit which decides when a particular step shall be taken, and the function staticizors which decide what steps shall be taken. Waveforms from these two parts are taken to all parts of the machine to control their operation.

Let us consider the sequence of steps in obeying an instruction. We will assume that the new instruction is just emerging from the store. It is sent to the instruction or 1

register, a single word regenerative track, to be stored. A facility is available whereby this instruction may be modified before it is actually obeyed. This is one of the functions of the B store, which can have numbers from the main store transferred to, or subtracted from, its 8 addresses. Instructions which need modifying use their B digits to specify which of the 8 B store addresses should be used. If an instruction has any combination of digits, except three zero's, in the B digit position, and does not call for an operation involving a B store, that instruction will be modified by having the contents of the B address specified in the instruction, added to it before it is obeyed.

If modification of the instruction is called for the instruction is fed out of the I register to the arithmetic unit, together with the contents of the relevant B store and the sum is put back into the I register. The function digits in the instruction register, P4 to P8 in S0, now set up the coded function staticizors which in turn through a diode matrix, set up one of the 26 function staticizors which determine which operation will be performed. At the same time the digits P6 to P11 in S1 in the instruction register set the coded track staticizors which through another diode matrix, select the track required.

The actual operation to be performed has now been determined and in general it involves first, searching for a number in the store or in a register. This number is then stored in the E register while a search for the other number

or address needed takes place. When this is located the arithmetic operation takes place and the answer is placed in the second address. Now the coded track staticizors are reset by P6 to P11 in S2 of the instruction register and the next instruction which is in the address specified in S2 of the instruction register is searched for. When this appears the whole sequence is repeated. Had the instruction been one calling for the examination of a sign or a multiplication, the procedure, after placing the number in the E register, would have been slightly different. In the case of examining a sign, the number which is to be examined, which is either in the accumulator or is in one of the B addresses, is put into the E register as before. Then the sign of it is examined and depending on the result, the search for the next instruction takes place either using the address in S1 or the one in S2 of the I register.

If a multiplication was called for, the number put into the E register would be the multiplier. No further search is necessary as the multiplicand will have already been put into the D register, and so the procedure of successive shift is carried out as explained in the previous section, until all the one's in the E register have been examined. The multiplication is now complete and the next instruction is found as before by searching for the address in S2 of the instruction register.

3.6 Input and Output

Input to the machine is by means of standard 5 hole punched paper tape which is read at up to 200 rows per second by a high speed photo electric reader. The reader, controlled

by the computer, sets the 5 input staticizors which are sampled to give a serial output suitable for reading into the store. Decimal numbers are represented by punching a five hole combination on the tape for each decimal digit. These combinations are arranged to be the binary equivalents of the decimal digits. The input routine of the computer converts this binary coded decimal representation of the number into its true binary form.

Two forms of output are provided, punched paper tape, and a printed copy. A switch selects either or both. The punched tape output has a maximum speed of 25 rows per second and the printer the maximum speed of 7 characters per second. Thus it is better to use the punch if the high speed is required but the printer is invaluable when programmes are being checked and intermediate results need to be examined quickly.

### 3.7 Operating Controls and Monitoring Facilities

The operator sits at a control desk which has all the controls and displays on it that he needs. The computer is started by pressing the "start" button and it then proceeds under the control of a three position key. The postions of this key are "auto", "single instruction", and "single coincidence". In the "auto" position instructions are obeyed at high speed until either a "stop" instruction appears or the key is changed to another position. In the "single instruction" position, instructions are obeyed singly each time the "start" button is pressed. In the "single coincidence" position, each instruction is obeyed in three stages, the "start" button again being depressed at each stage. A special stop instruction is provided which only

stops the machine if the "stop" key is depressed, otherwise the instruction is ignored.

Keys are provided which when pressed in one direction, clear the B store, the A, E, I, and M, register respectively and, except in the case of the B store, when pressed in the other direction cause the number set on the hand switches to be placed in that register.

The hand switches are a set of 36 keys which enable any number or instruction to be manually set up and placed in any of the registers. The contents of each register may be examined on one of the two cathode ray tubes displays provided on the control desk, by means of a rotating selector switch. The other display shows, by means of a suitable raster, either the contents of the B store, or the contents of one track of the main store. The actual track displayed is selected by setting its track number in binary code on the 7 keys provided.

3.8 Power Supplies

The power for the computer will be provided by a motor alternator set which will remove all transients and short term failures from the a.c. supply. The total power consumption will be about 2 kW.

D.C. supplies for the transistor circuitry are provided by metal rectifier units and provision is made to vary the positive supply of 30 volts for marginal testing purposes. The valve heaters are capable of being switched on in two stages to prevent the initial high current which otherwise occurs. H.T. supplies for the valve circuits are provided by rectifier units

producing + 600 volts, + 300 volts, + 150 volts, and - 150 volts, the + 300 volts supply being stabilised. An interlock system is provided so that failure of any one supply will cause other supplies liable to cause damage to be switched off.

## Appendix 1

## Specification of Type 950 Digital Computer

The computer is designed for general purpose use, for both manual and automatic operation.

| | |
|---|---|
| Clock Frequency | 57.5 Kc/s. |
| Number Base | External, 10. Internal, 2. |
| Word Length | 32 binary digits. |
| Instruction Code | Approximately 26 one address instructions including addition, subtraction, multiplication, logical operations. |
| Arithmetic Unit | Serial Mode. |
| Storage | (a) 8 'B' stores.<br>(b) Main store for 4,096 words, mean access time 10 Msec.<br>These are combined on one magnetic drum. |
| Input/Output Mechanisms — Input | Keyboard - manual, tape reader - automatic, at 200 rows per sec. |
| Output | C.R.T. display - direct reading (binary), teleprinter - automatic, at 7 characters/sec., tape punch - automatic, at 25 rows/sec. |
| Speed | Addition, subtraction, and transfer - 3.45Msec.<br>Multiplication - 40 Msec. |

These items assume optimum programming has been used. Otherwise they should both be increased by 20 Msec.

## Appendix 2

## Digital Computer Type 950

### Instruction Code

Arithmetic

| | | |
|---|---|---|
| F0 | Clear Accumulator | A' = 0 |
| F1 | Add contents of store locn. S to Accumulator. | A' = A + S |
| F2 | Subtract contents of store locn. S from Accumulator | A' = A - S |
| F3 | Add contents of store locn. S to the most significant part of the Accumulator | M' = M + S |
| F4 | Transfer number in store locn. S to Multiplicand register | D' = S |
| F5 | Multiply store locn. S by D and add the product to the Accumulator | A' = A + DS. |
| F6 | Multiply store locn. S by D and subtract the product from the Accumulator | A' = A - DS. |
| F7 | Transfer number in the least significant part of the Accumulator to store locn. S | S' = L |
| F8 | Transfer number in the most significant part of the Accumulator to store locn. S | S' = M |
| F9 | Shift the Accumulator contents x places to the right | $A' = 2^{x}A.$ |
| F10 | Shift the Accumulator contents x places to the left | $A' = 2^{-x}A$ |
| F11 | Transfer Random number to the least significant part of the Accumulator | |

B. Store

| | | |
|---|---|---|
| F12 | Transfer number in store locn. S to B store | B' = S |
| F13 | Transfer number in B store to store locn. S | S' = B |
| F14 | Subtract number in store locn. S from B store | B' = B - S |

Appendix 2 (continued)

Logical

| | | |
|---|---|---|
| F15 | Discriminate on the sign of the Accumulator | |
| F16 | Discriminate on the sign of the B store | |
| F17 | Collate contents of store locn. S with least significant part of Accumulator and place result in least significant part of Accumulator | L' = L & S |
| F18 | Perform logical operation 'or' with store locn. S and least significant part of Accumulator and place result in least significant part of Accumulator | L' = L"or"S |

Control

| | | |
|---|---|---|
| F19 | Place the contents of the hand switches in store locn. S | S' = H.S. |
| F20 | Stop if stop key depressed | |
| F21 | Stop | |

Input

| | |
|---|---|
| F22 | Place five digits from input tape in five most significant digits of the Accumulator |

Output

| | |
|---|---|
| F23 | Punch or print out five most significant digits of the Accumulator. |
| F24 | Space printer |
| F25 | Line Feed |
| F26 | Carriage return. |

The product of two single length numbers will be a double length number. These numbers expressed in double length form are:-

$$R_{2Q} = \left\{ \sum_{0}^{2Q-1} R_q 2^q - R_{2Q-1} 2^{2Q} \right\} \quad \text{the multiplier}$$

$$D_{2Q} = \left\{ \sum_{0}^{2Q-1} D_q 2^q - D_{2Q-1} 2^{2Q} \right\} \quad \text{the multiplicand.}$$

The product is given by:-

$$R_{2Q}D_{2Q} = \left\{ \sum_{0}^{Q-1} R_q 2^q + \sum_{Q}^{2Q-1} R_q 2^q - R_{2Q-1} 2^{2Q} \right\} \quad X$$

$$\left\{ \sum_{0}^{Q-1} D_q 2^q + \sum_{Q}^{2Q-1} D_q 2^q - D_{2Q-1} 2^{2Q} \right\}$$

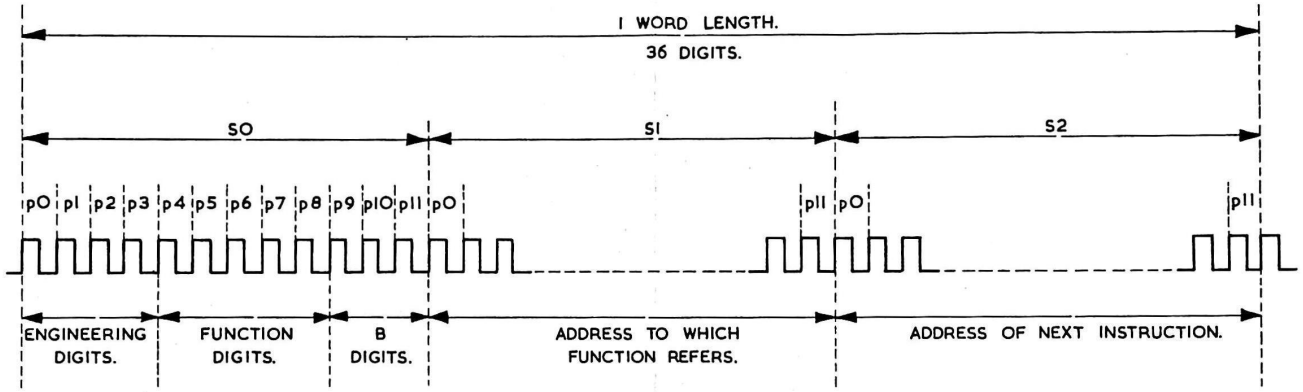
Now $$\sum_{Q}^{2Q-1} A_q 2^q = A_{2Q-1} 2^{2Q} - A_{Q-1} 2^Q$$

$$= A_{Q-1}(2^{2Q} - 2^Q)$$

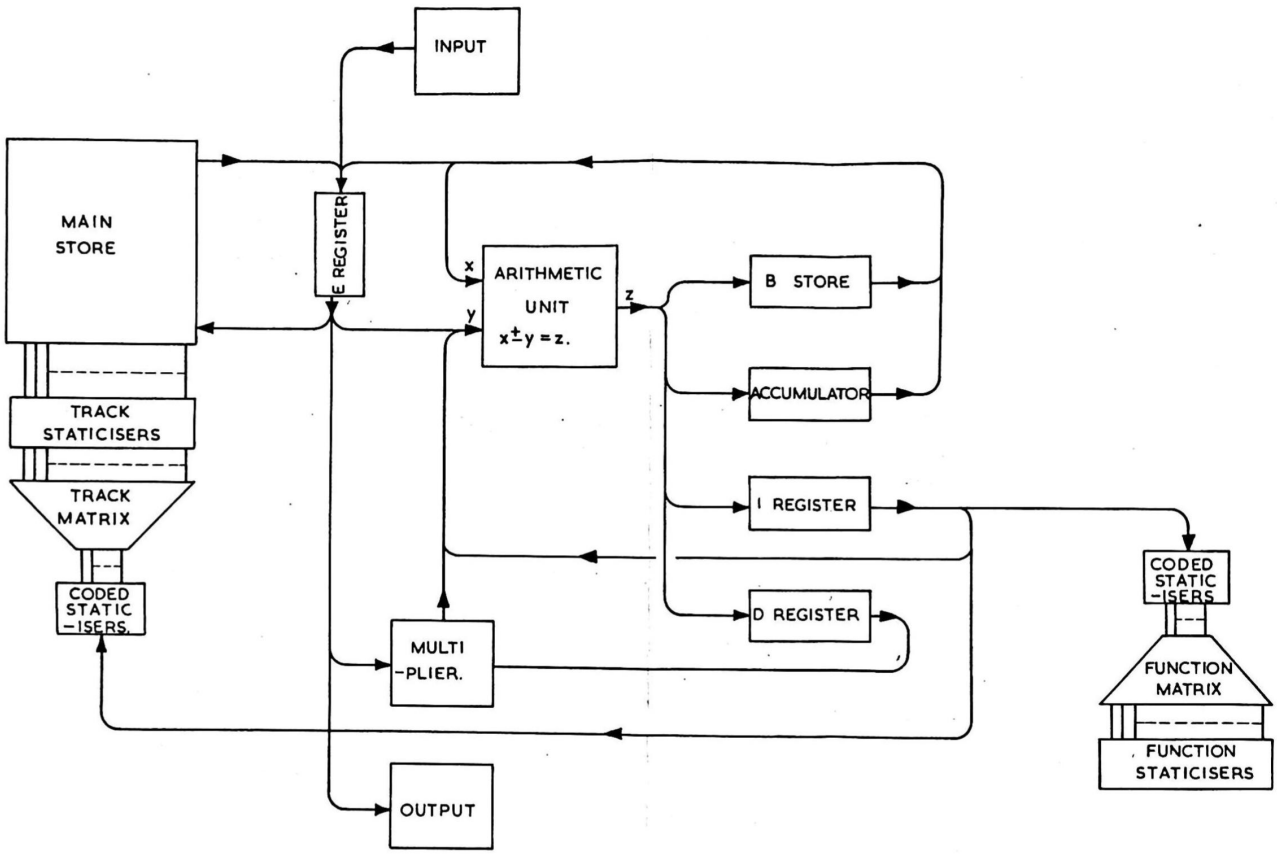
$$\therefore \quad R_{2Q}D_{2Q} = \left\{ \sum_{0}^{Q-1} R_q 2^q - R_{Q-1} 2^Q \right\} x \left\{ \sum_{0}^{Q-1} D_q 2^q - D_{Q-1}(2^{2Q} - 2^Q) \right\}$$

$$= \left\{ \sum_{0}^{Q-2} R_q 2^q - R_{Q-1} 2^{Q-1} \right\} x \left\{ \sum_{0}^{Q-1} D_q 2^q + D_{Q-1}(2^{2Q} - 2^Q) \right\}$$

The contents of the second bracket are produced by extending the multiplicand to 64 digits in the D Register, (by copying the most significant digit). The product is formed by adding all the partial products $R_q 2^q D$ to the accumulator with the exception of the last, $R_{Q-1} 2^{Q-1} D$ which is subtracted.




| | | |
|---|---|---|
| METROPOLITAN-VICKERS ELEC. CO. LTD. ENGINEERING REPORT Nº 1026. PART 1. | TYPE 950 COMPUTER. CONSTRUCTION OF AN INSTRUCTION. | FIG. 1. |

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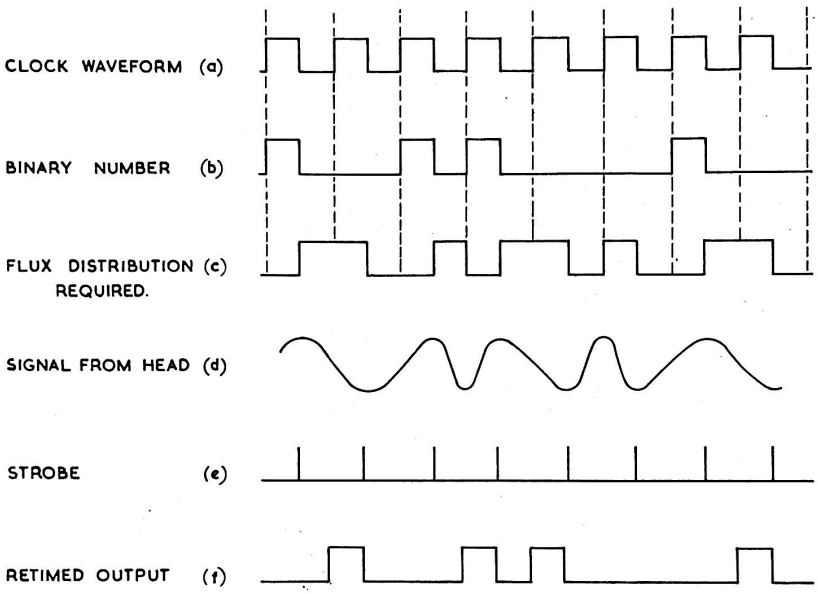
Nº 1026. PART. I.

TYPE 950 COMPUTER.
SIMPLIFIED BLOCK DIAGRAM.

FIG. 2.

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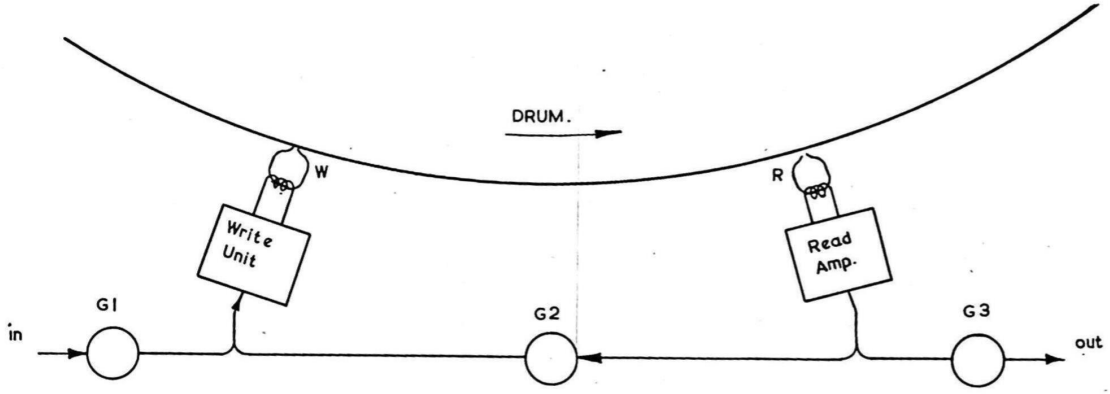
|---|---|---|
| METROPOLITAN-VICKERS ELEC. Co. LTD. ENGINEERING REPORT No. 1026. PART 1. | TYPE 950 COMPUTER WAVEFORMS IN THE MAGNETIC STORAGE SYSTEM. | FIG. 3. |

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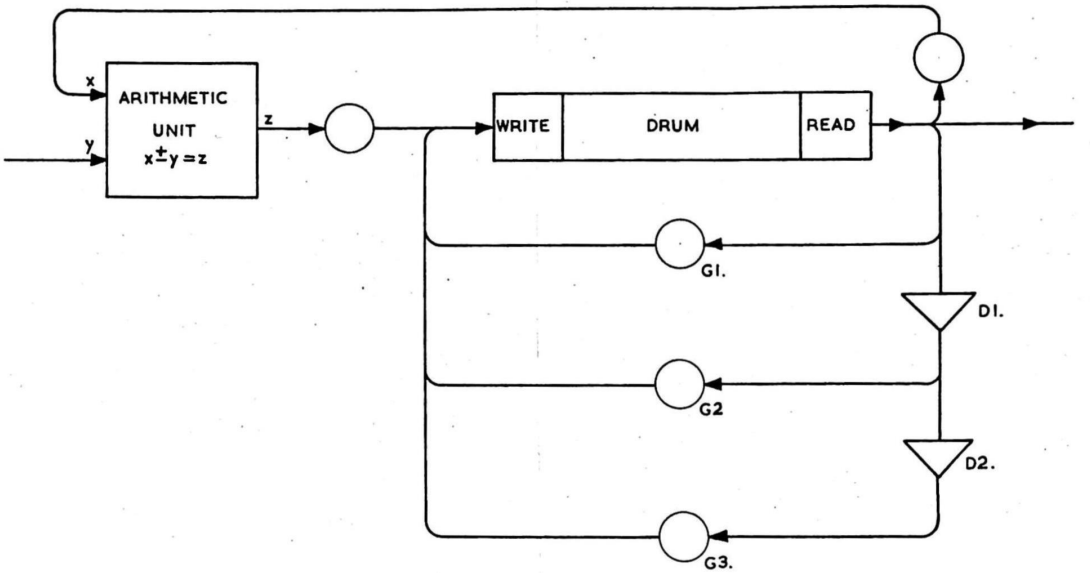
|---|---|---|
| METROPOLITAN VICKERS ELEC. CO. LTD. ENGINEERING REPORT No. 1026 PART 1. | TYPE 950 COMPUTOR. DIAGRAMMATIC REPRESENTATION OF A REGENERATIVE TRACK. | FIG. 4. |

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|---|---|---|
| METROPOLITAN-VICKERS ELEC. CO. LTD. ENGINEERING REPORT Nº 1026. PART. I. | TYPE 950 COMPUTER. THE ACCUMULATOR. | FIG. 6. |


VERDIVER 950